NEC

MOS INTEGRATED CIRCUIT

μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A)

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

Compared to the μPD78018F (standard model), the μPD78018F(A) employs a stricter quality-assurance program. (NEC calls this quality grade "special grade").

The μPD78018F(A) is a product in the μPD78018F subseries within the 78K/0 series.

Compared with the older μPD78014 subseries, this subseries operates at lower voltage and provides a fuller set of ROM and RAM variations.

A one-time PROM model μPD78P018F(A) capable of operating in the same power supply voltage as of the mask ROM product and other development tools are also provided.

Functions are described in detail in the following User's Manual, which should be read when carring out design work.

μPD78018F, 78018FY Subseries User's Manual : U10659E
78K/0 Series User's Manual – Instruction : U12326E

FEATURES

- Large on-chip ROM & RAM

Item / Product Name	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Internal Expanded RAM	Buffer RAM	
μPD78011F(A)	8K bytes	512 bytes	–	32 bytes	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm)
μPD78012F(A)	16K bytes				
μPD78013F(A)	24K bytes	1024 bytes			
μPD78014F(A)	32K bytes				
μPD78015F(A)	40K bytes		512 bytes		
μPD78016F(A)	48K bytes				
μPD78018F(A)	60K bytes		1024 bytes		

- External memory expansion space: 64K bytes
- Minimum instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 53 (N-ch open-drain: 4)
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 2 channels
- Timer: 5 channels
- Supply voltage: V_{DD} = 1.8 to 5.5 V

In addition to the μPD78011F(A), 78012F(A), 78013F(A), 78014(A), 78015F(A), 78016F(A), and 78018F(A), this document also describes μPD78012F(A2). However, unless otherwise specified, the μPD78018F(A) is treated as the representative model throughout this document.

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The mark ★ shows major revised points.

APPLICATION

Control unit of automotive, gas leak breaker, and safety devices, etc.

ORDERING INFORMATION

Part Number	Package
μPD78011FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78011FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78012FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78012FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
★ μPD78012FGC (A2)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78013FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78013FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78014FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78014FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78015FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78015FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78016FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78016FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78018FCW (A)-×××	64-pin plastic shrink DIP (750 mil)
μPD78018FGC (A)-×××-AB8	64-pin plastic QFP (14 × 14 mm)

Remark ××× indicates a ROM code suffix.

QUALITY GRADE

Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

DIFFERENCES BETWEEN STANDARD MODEL AND (A) MODELS

Item \ Product Names	(A) Models	Standard Model
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)
Quality grade	Special	Standard

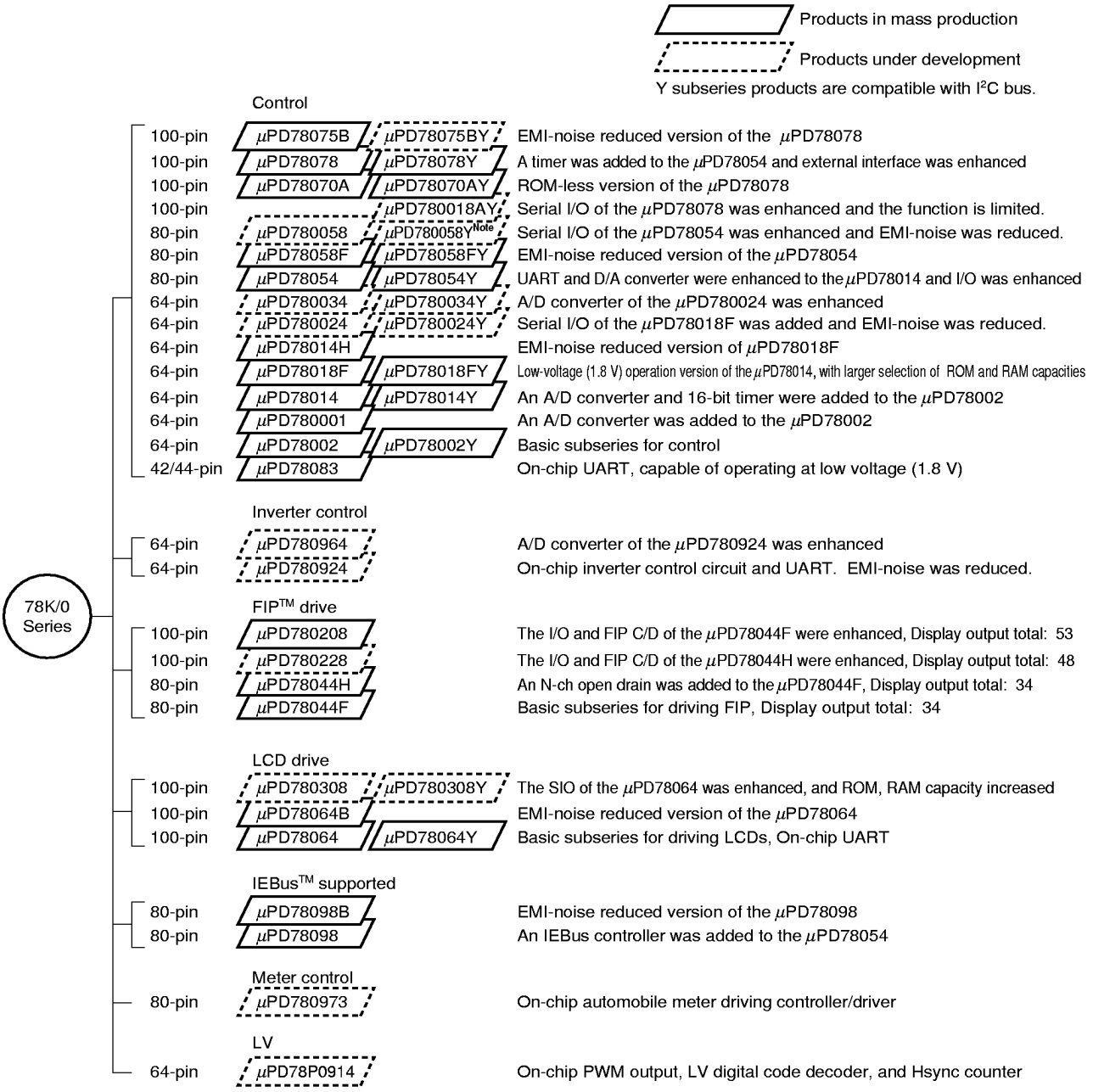
★ DIFFERENCES BETWEEN μPD78012F(A) AND μPD78012F(A2)

Item \ Product Names	μPD78012F(A)	μPD78012F(A2)
Supply voltage	V_{DD} = 1.8 to 5.5 V	V_{DD} = 5 V ± 10 %
Operating temperature	T_A = –40 to +85 °C	T_A = –40 to +125 °C
Minimum instruction execution time	0.4 μs (at 10-MHz operation)	0.5 μs (at 8-MHz operation)
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm)	• 64-pin plastic QFP (14 × 14 mm)

Remark In addition to the above, the supply voltage and so on are different. For details, refer to **11. ELECTRICAL SPECIFICATIONS**.

★ **78K/0 Series Expansion**

The following shows the 78K/0 Series products development. Subseries name are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K-40K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	88	1.8 V	○
	μPD78078	48K-60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24K-60K	2ch						2ch	3ch (time division UART: 1ch)	68	1.8 V	
	μPD78058F	48K-60K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16K-60K										2.0 V	
	μPD780034	8K-32K					–	8ch	–	3ch (UART: 1ch, time division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53	1.8 V	
	μPD78018F	8K-60K											
	μPD78014	8K-32K										2.7 V	
	μPD780001	8K		–	–					1ch	39		–
	μPD78002	8K-16K			1ch		–				53		○
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter control	μPD780964	8K-32K	3ch	**Note**	–	1ch	–	8ch	–	2ch (UART: 2ch)	47	2.7 V	○
	μPD780924						8ch	–					
FIP drive	μPD780208	32K-60K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48K-60K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32K-48K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16K-40K								2ch			
LCD drive	μPD780308	48K-60K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time division UART: 1ch)	57	2.0 V	–
	μPD78064B	32K								2ch (UART: 1ch)			
	μPD78064	16K-32K											
IEBus supported	μPD78098B	40K-60K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	69	2.7 V	○
	μPD78098	32K-60K											
Meter control	μPD780973	24K-32K	3ch	1ch	1ch	1ch	5ch	–	–	2ch (UART: 1ch)	56	4.5 V	–
LV	μPD78P0914	32K	6ch	–	–	1ch	8ch	–	–	2ch	54	4.5 V	○

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTION

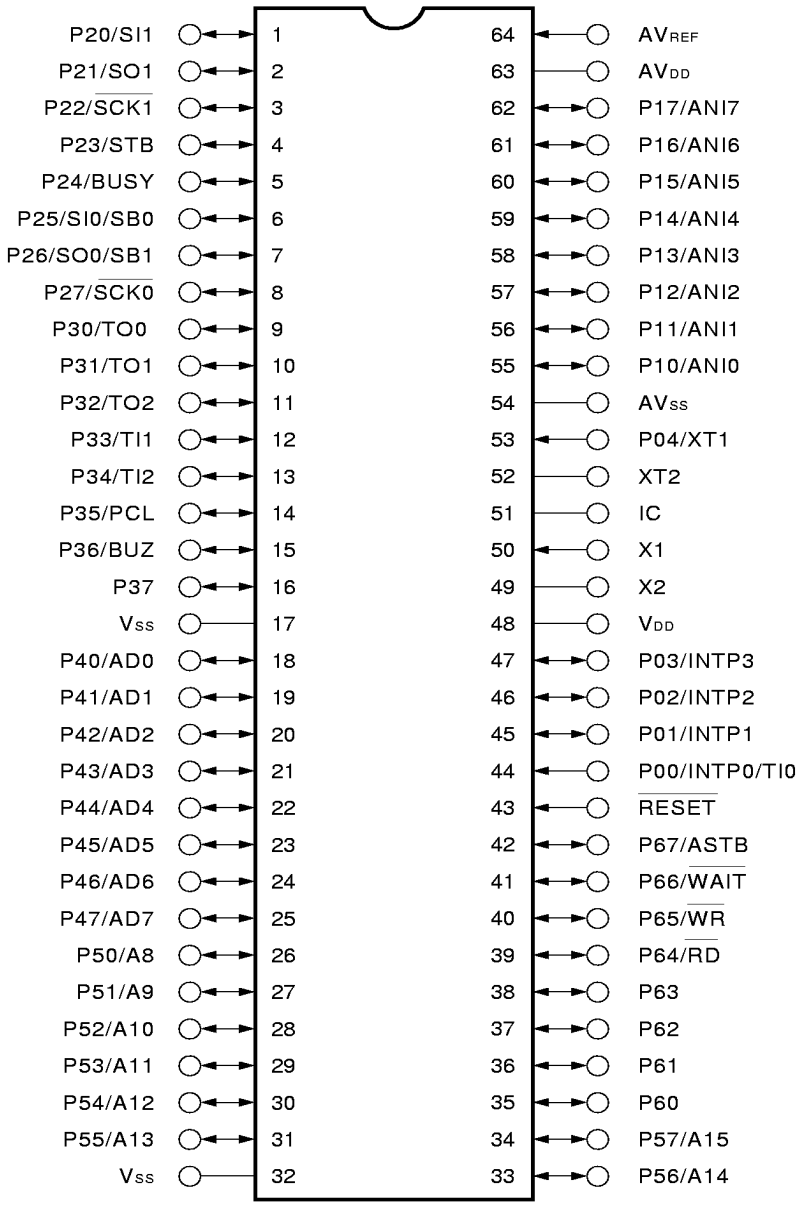
Item \ Product Name		μPD78011F(A)	μPD78012F(A)	μPD78013F(A)	μPD78014F(A)	μPD78015F(A)	μPD78016F(A)	μPD78018F(A)
Internal memory	ROM	8K bytes	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	60K bytes
	High-speed RAM	512 bytes		1024 bytes				
	Expanded RAM	–				512 bytes		1024 bytes
	Buffer RAM	32 bytes						
Memory space		64K bytes						
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)						
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function						
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)						
	When subsystem clock selected	122 μs (at 32.768 kHz operation)						
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.						
I/O ports		Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4						
A/D converter		• 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: AV_{DD} = 1.8 to 5.5 V						
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel						
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel						
Timer output		3 (14-bit PWM output × 1)						
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock 10.0 MHz operation), 32.768 kHz (at subsystem clock 32.768 kHz operation)						
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 10.0 MHz operation)						
Vectored interrupt sources	Maskable	Internal: 8, External: 4						
	Non-maskable	Internal: 1						
	Software	1						
Test input		Internal: 1, External: 1						
Supply voltage		V_{DD} = 1.8 to 5.5 V						
Operating ambient temperature		T_A = –40 to +85 °C						
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm)						

★ **Caution Compared to the other models, the μPD78012F(A2) differs in terms of the voltage and supply current. Refer to DIFFERENCES BETWEEN μPD78012F(A) AND μPD78012F(A2).**

CONTENTS

1. PIN CONFIGURATION (Top View)

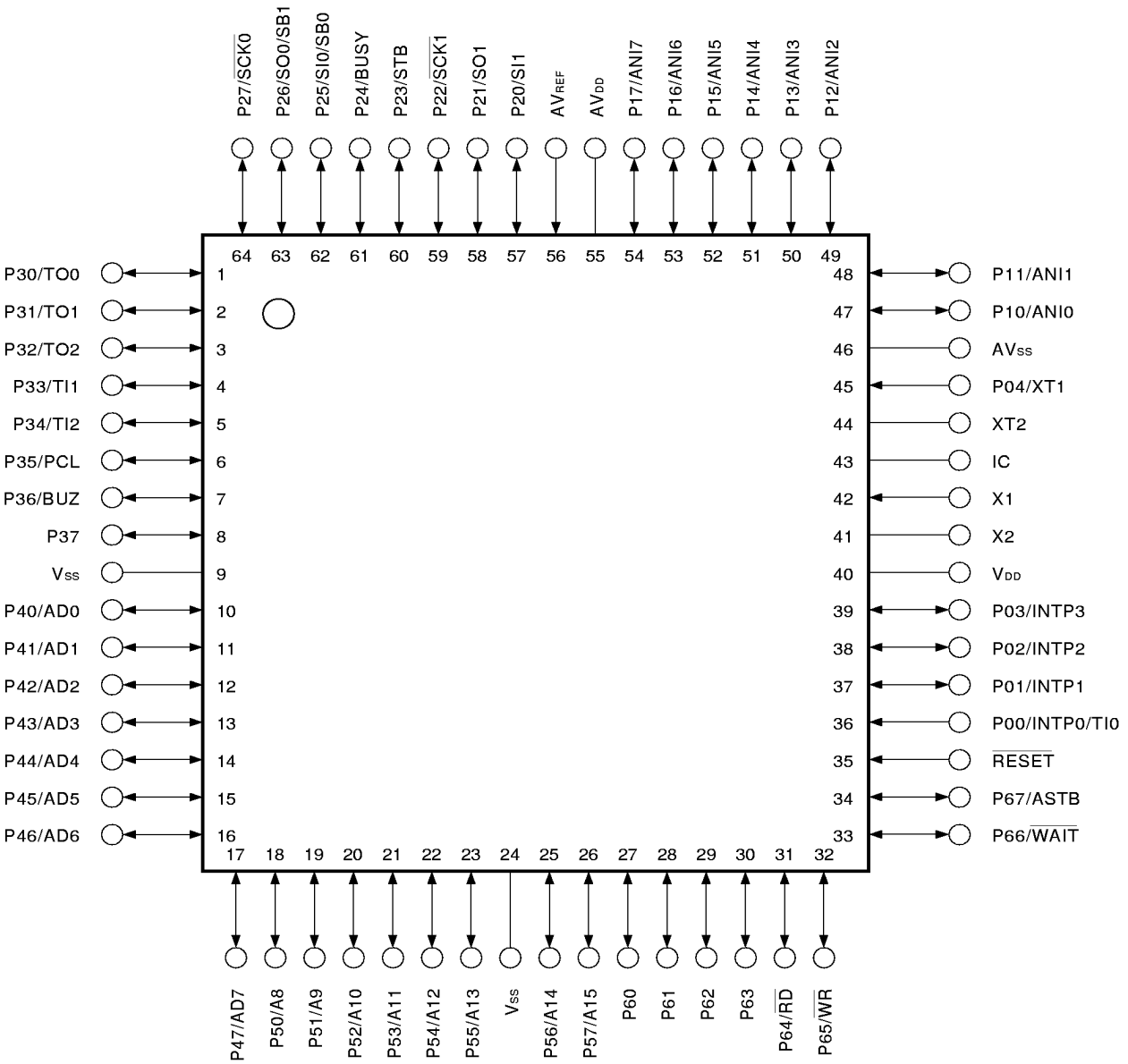
- **64-Pin Plastic Shrink DIP (750 mil)**
  μPD78011FCW(A)-×××, 78012FCW(A)-×××, 78013FCW(A)-×××,
  μPD78014FCW(A)-×××, 78015FCW(A)-×××, 78016FCW(A)-×××, 78018FCW(A)-×××



Cautions 1. Always connect the IC (Internally Connected) pin to V_{SS} directly.
2. Always connect the AV_{DD} pin to V_{DD}.
3. Always connect the AV_{SS} pin to V_{SS}.

- **64-Pin Plastic QFP (14 × 14 mm)**

★ **μPD78011FGC(A)-×××-AB8, 78012FGC(A)-×××-AB8, 78012FGC(A2)-×××-AB8, 78013FGC(A)-×××-AB8, μPD78014FGC(A)-×××-AB8, 78015FGC(A)-×××-AB8, 78016FGC(A)-×××-AB8, 78018FGC(A)-×××-AB8**



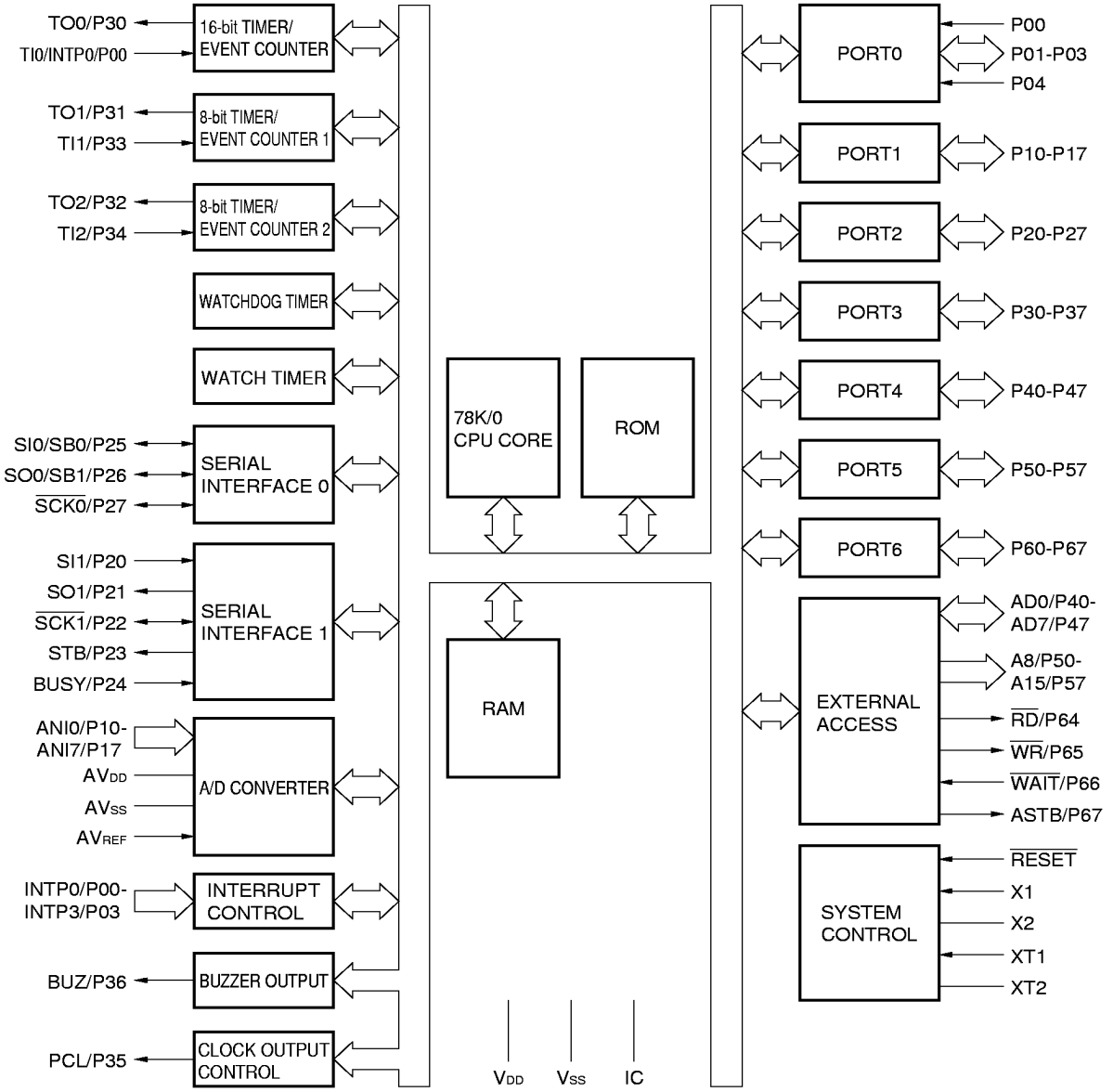
Cautions 1. Always connect the IC (Internally Connected) pin to V_{SS} directly.

2. Always connect the AV_{DD} pin to V_{DD}.

3. Always connect the AV_{SS} pin to V_{SS}.

A8 to A15	:	Address Bus
AD0 to AD7	:	Address/Data Bus
ANI0 to ANI7	:	Analog Input
ASTB	:	Address Strobe
AV_{DD}	:	Analog Power Supply
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
BUSY	:	Busy
BUZ	:	Buzzer Clock
IC	:	Internally Connected
INTP0 to INTP3	:	Interrupt from Peripherals
P00 to P04	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
PCL	:	Programmable Clock
$\overline{RD}$	:	Read Strobe
$\overline{RESET}$	:	Reset
SB0, SB1	:	Serial Bus
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock
SI0, SI1	:	Serial Input
SO0, SO1	:	Serial Output
STB	:	Strobe
TI0 to TI2	:	Timer Input
TO0 to TO2	:	Timer Output
V_{DD}	:	Power Supply
V_{SS}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark Internal ROM & RAM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.[Note 2]		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P04/XT1 pins as an input port, set 1 to bit 6 (REC) of the processor clock control register (PCC). Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, on-chip pull-up resistor is automatically unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, on-chip pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

3.2 OTHER PORTS (1/2)

Pin Name	I/O	Function	On Reset	Dual-Function Pin
INTP0	Input	External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt request input.		P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SB0	Input/output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output.	Input	P27
$\overline{SCK1}$				P22
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24

3.2 OTHER PORTS (2/2)

Pin Name	I/O	Function	On Reset	Dual-Function Pin
TI0	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connected to V_{SS} directly.	—	—

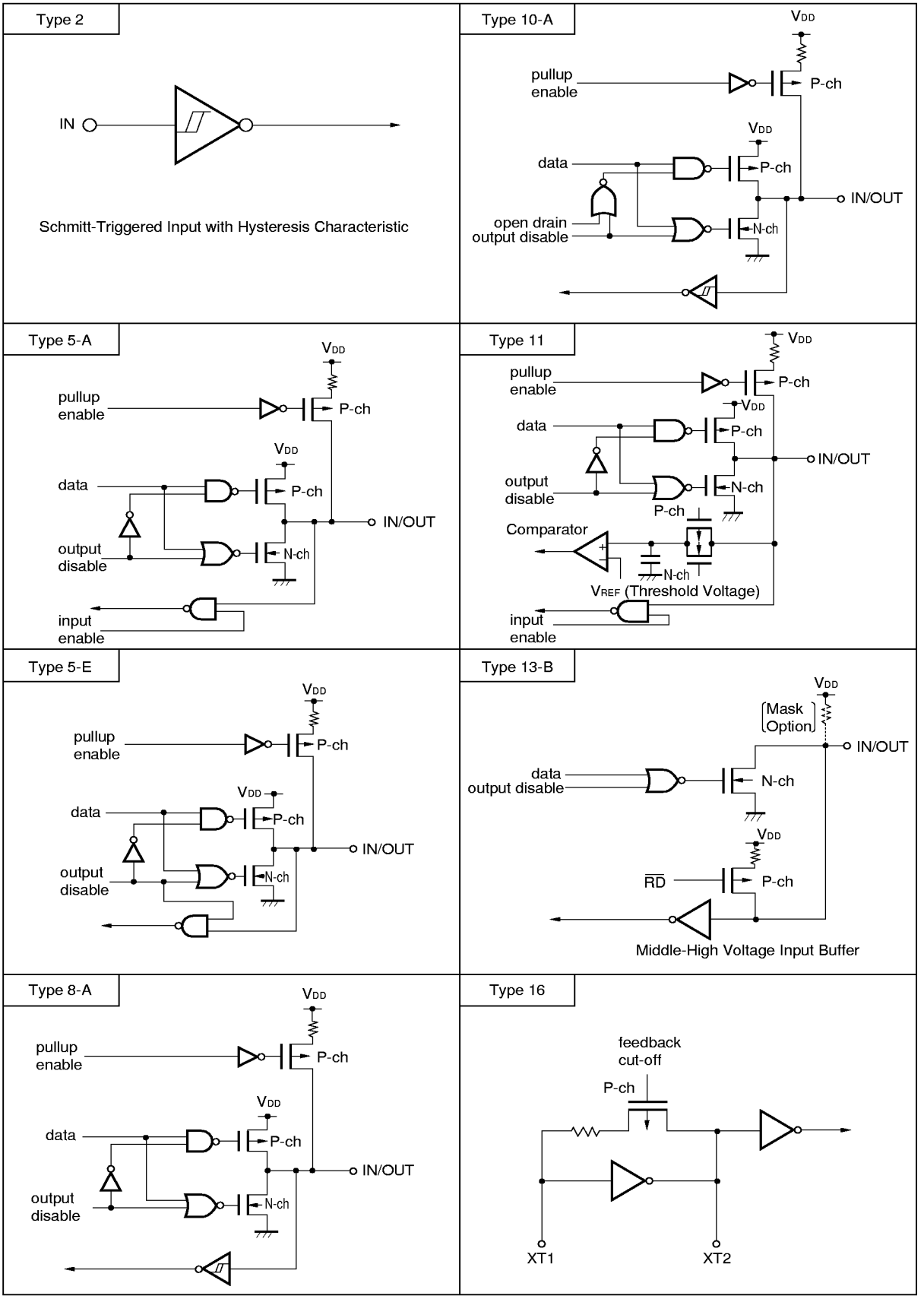
3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0/TI0	2	Input	Connected to V_{SS}.
P01/INTP1	8-A	Input/output	Individually connected to V_{SS} via resistor.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to V_{DD} or V_{SS}.
P10/ANI0 to P17/ANI7	11	Input/output	Individually connected to V_{DD} or V_{SS} via resisitor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Individually connected to V_{DD} via resistor.
P50/A8 to P57/A15	5-A		Individually connected to V_{DD} or V_{SS} via resistor.
P60 to P63	13-B		Individually connected to V_{DD} via resistor.
P64/$\overline{RD}$	5-A		Individually connected to V_{DD} or V_{SS} via resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF}	—		Connected to V_{SS}.
AV_{DD}			Connected to V_{DD}.
AV_{SS}			Connected to V_{SS}.
IC			Connected to V_{SS} directly.

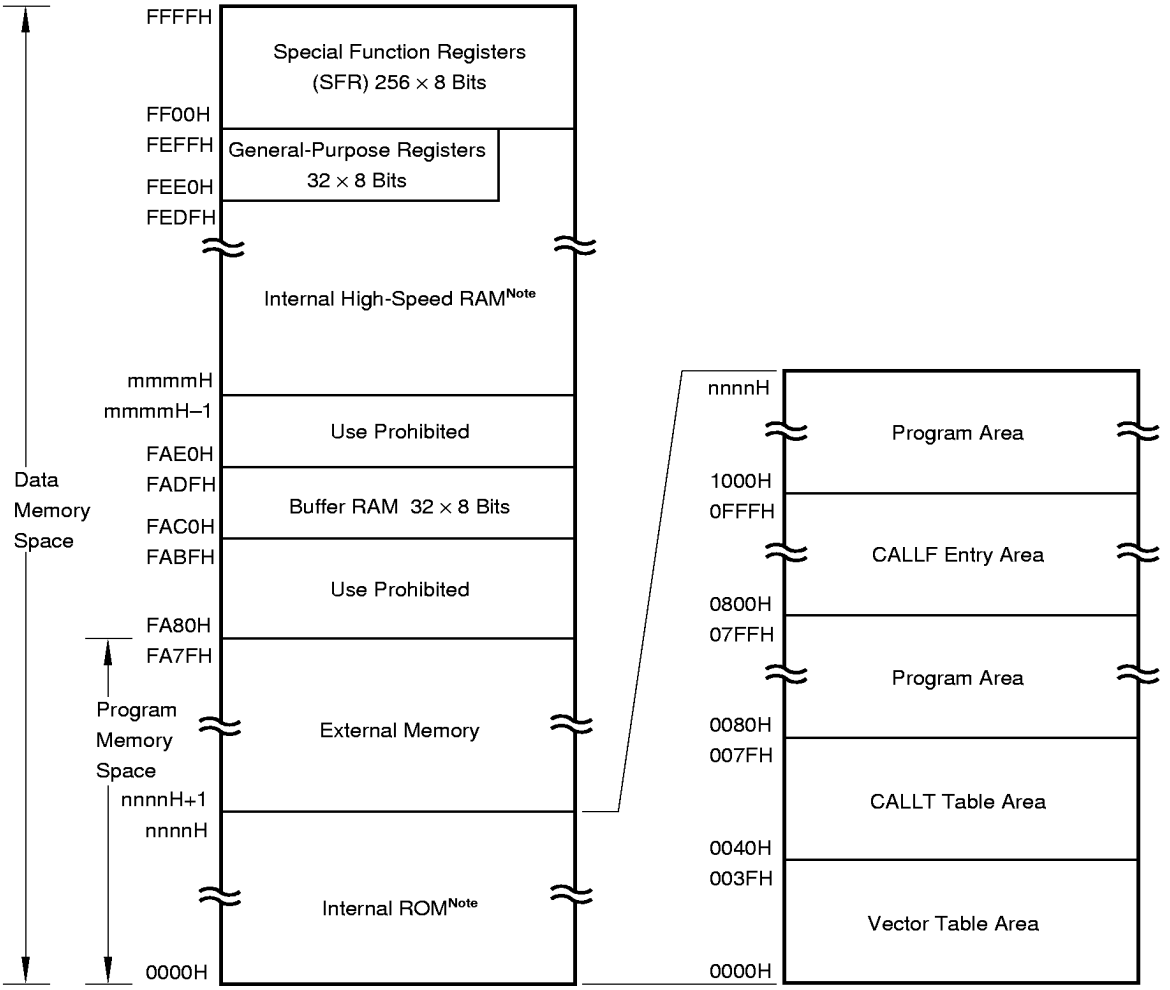
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), and 78018F(A) is shown in Figures 4-1 and 4-2.

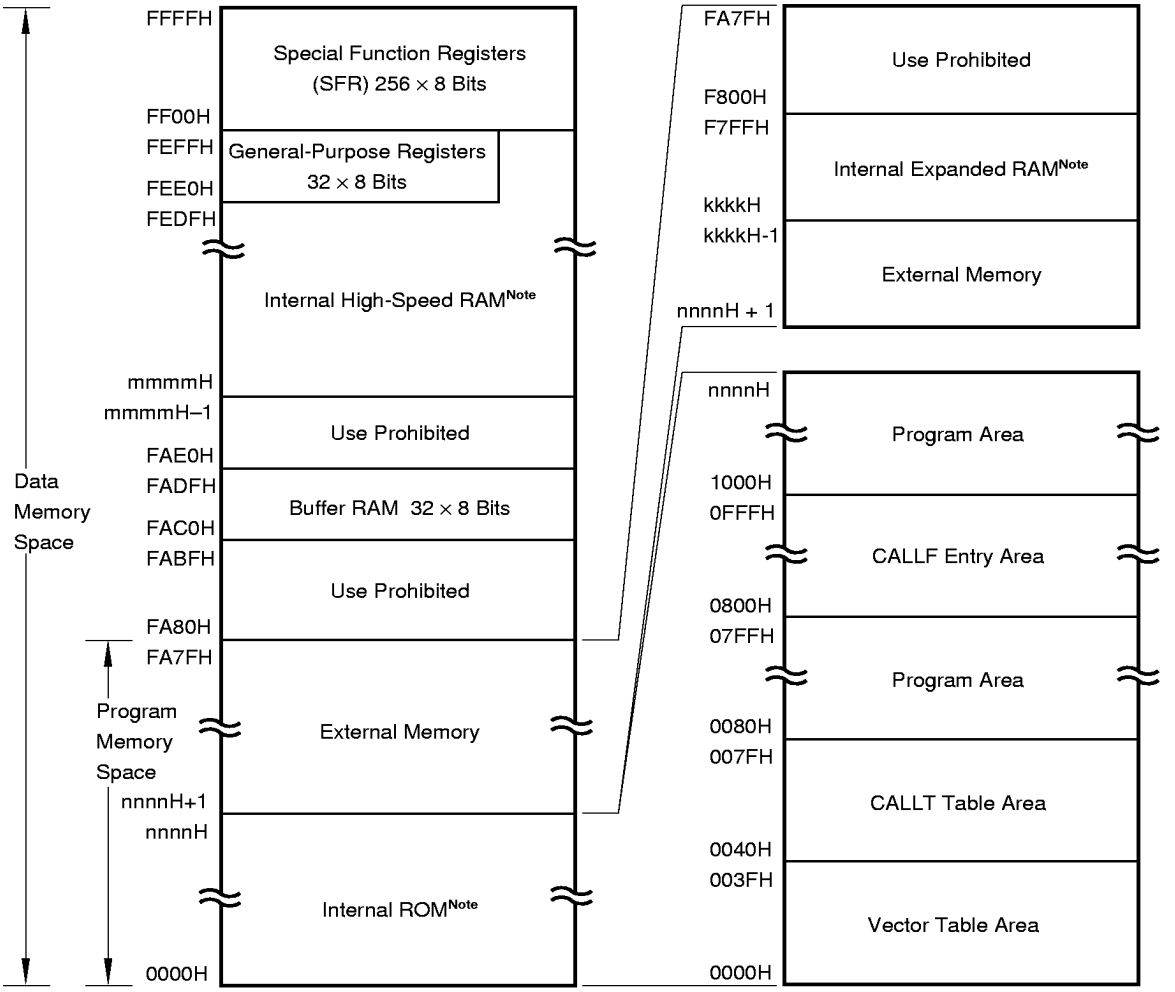
Figure 4-1. Memory Map (μPD78011F(A), 78012F(A), 78013F(A), 78014F(A))



Note Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

Product Name	Intenal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78011F(A)	1FFFH	FD00H
μPD78012F(A)	3FFFH	
μPD78013F(A)	5FFFH	FB00H
μPD78014F(A)	7FFFH	

Figure 4-2. Memory Map (μPD78015F(A), 78016F(A), 78018F(A))



Note Internal ROM, internal high-speed RAM and internal extended RAM capacities vary depending on the product (see the table below).

Product Name	Intenal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH	Internal Extended RAM Start Address kkkkH
μPD78015F(A)	9FFFH	FB00H	F600H
μPD78016F(A)	BFFFH		
μPD78018F(A)	EFFFH		F400H

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The I/O port has the following three types

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
- N-ch open-drain input/output(15V withstand voltage) (P60 to P63) : 4

Total : 53

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated Input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.

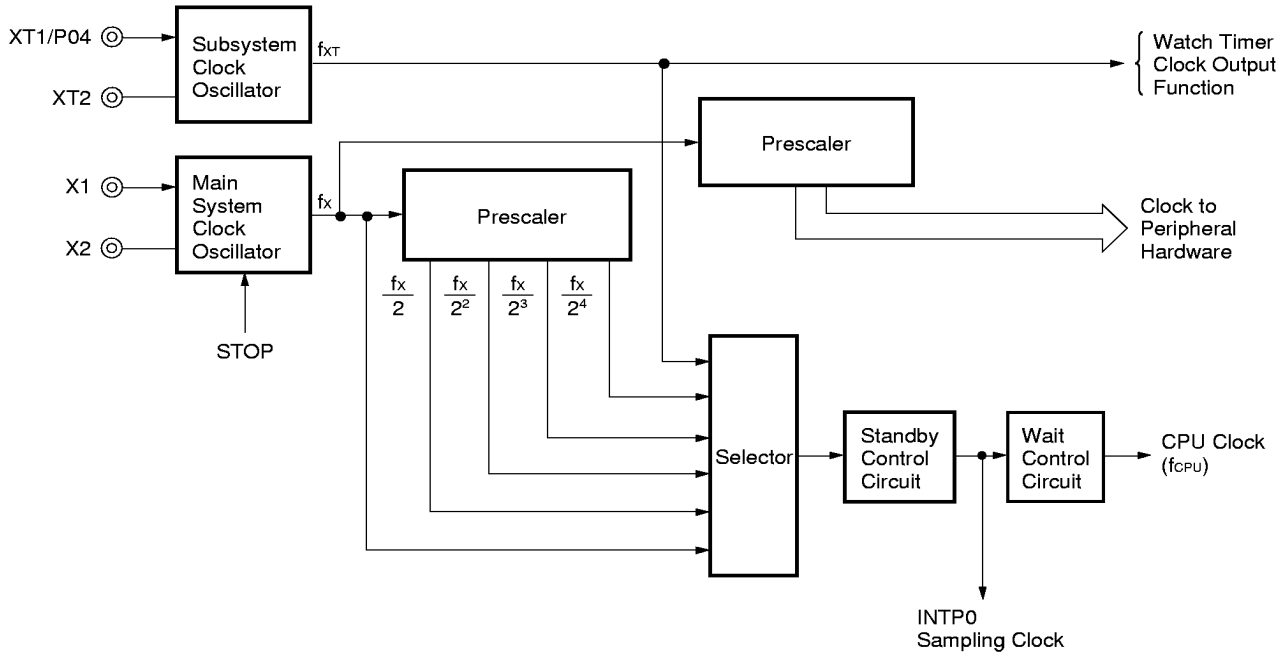
5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock.

The minimum instruction exection time can be changed.

- 0.4μs/0.8μs/1.6μs/3.2μs/6.4μs (Main system clock: at 10.0 MHz operation)
- 122μs (Subsystem clock: at 32.768 KHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

The following five channels are incorporated in the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counter

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1 channel	1 channel
	Externanal event counter	1 channel	2 channels	–	–
Functions	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width mesurement	1 input	–	–	–
	Sqare wave output	1 output	2 outputs	–	–
	Interrupt request	2	2	1	1
	Test input	–	–	1 input	–

Figure 5-2. 16-bit Timer/Enent Counter Block Diagram

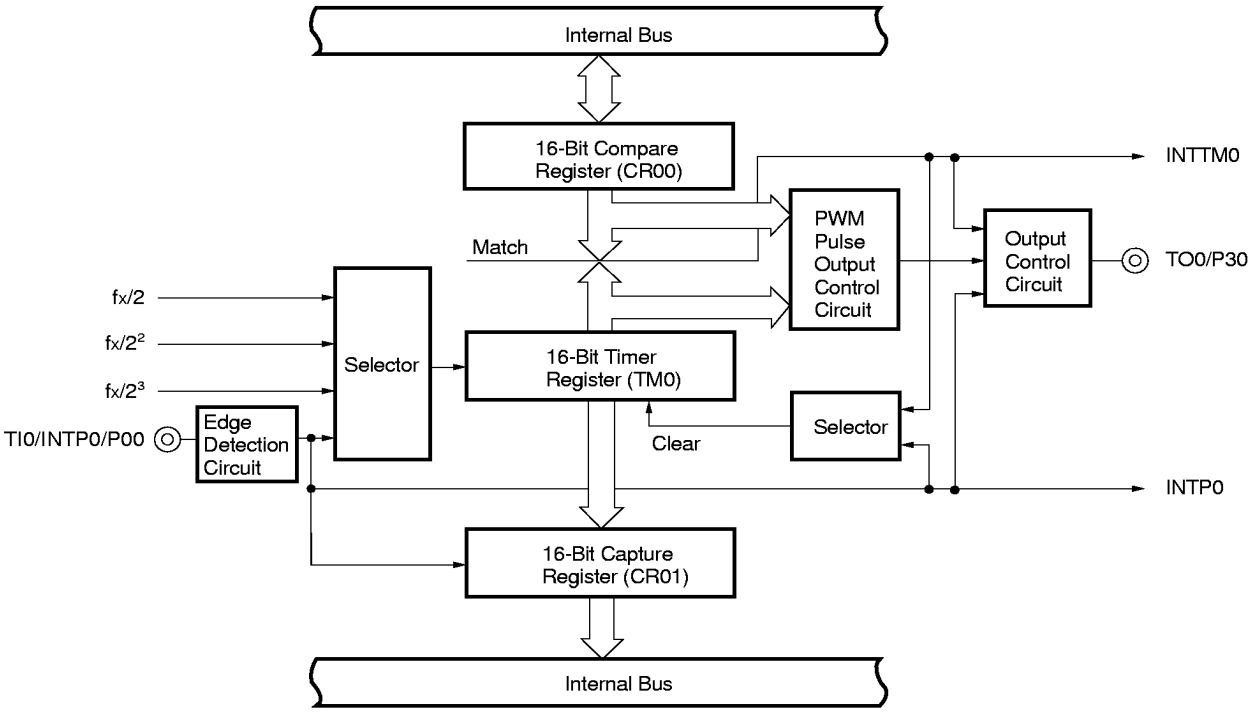


Figure 5-3. 8-bit Timer/Enent Counter Block Diagram

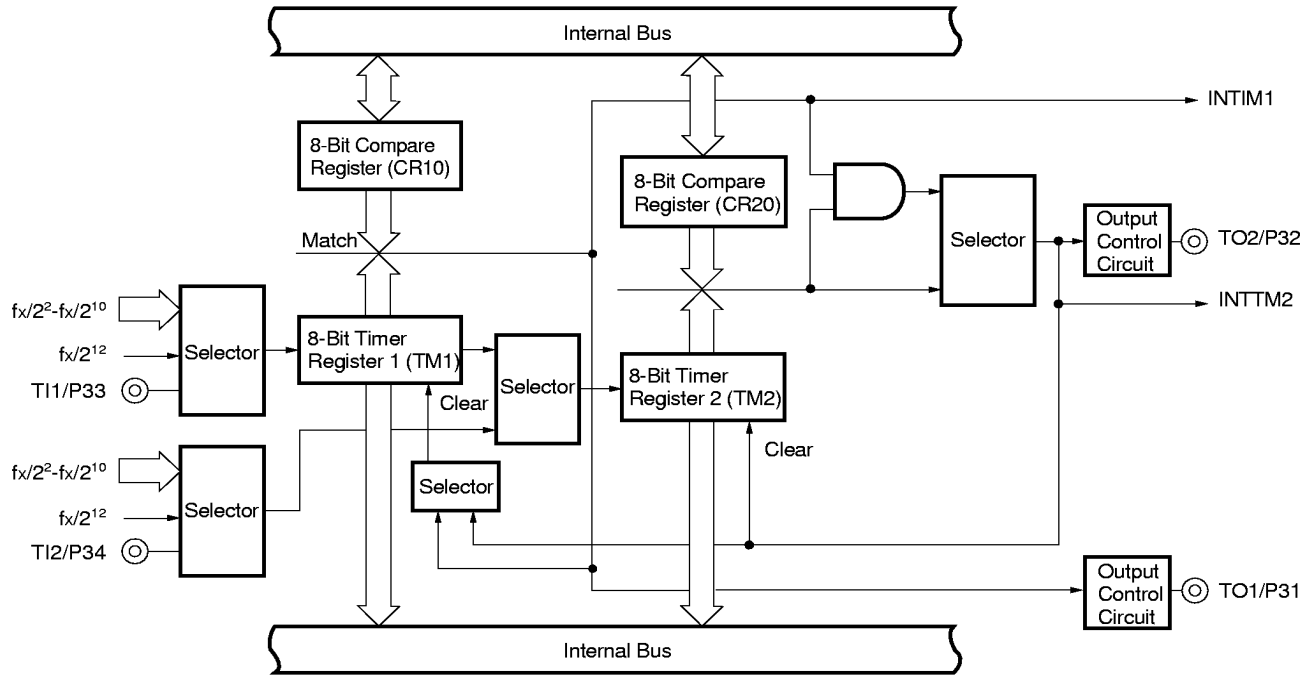


Figure 5-4. Watch Timer Block Diagram

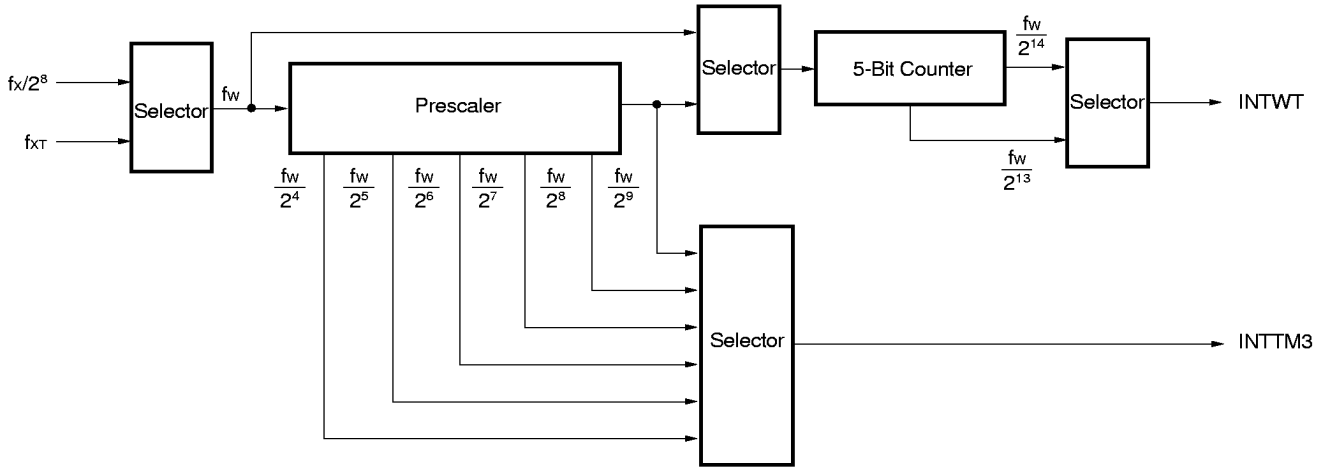
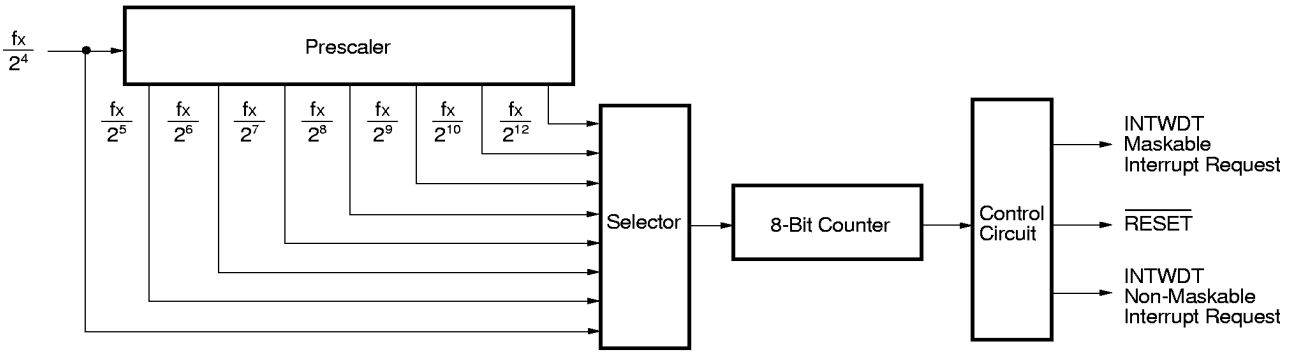


Figure 5-5. Watchdog Timer Block Diagram

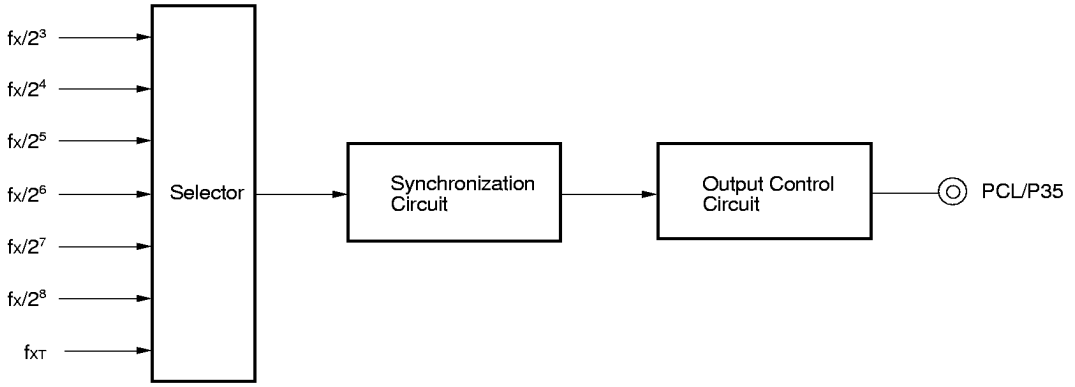


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Block Diagram

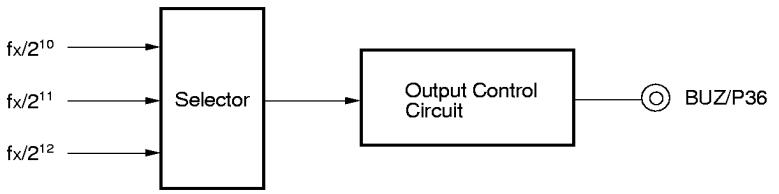


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Figure 5-7. Buzzer Output Control Block Diagram

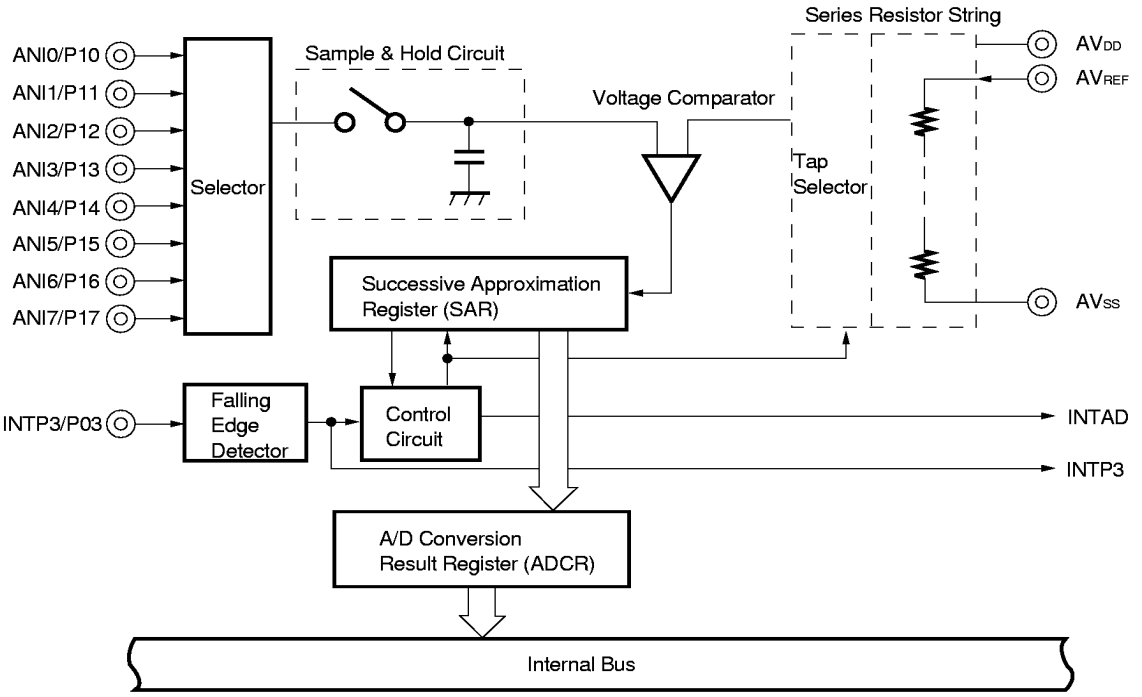


5.6 A/D CONVERTER

The A/D converter has on-chip eight 8-bit resolution channels.
There are the following two method to start A/D conversion.

- Hardware starting
- Software starting

Figure 5-8. A/D Converter Block Diagram



5.7 SERIAL INTERFACES

There are two on-chip clocked serial interfaces as follows.

- Serial Interface channel 0
- Serial Interface channel 1

Table 5-3. Type and Function of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	○ (MSB/LSB-first switchable)	○ (MSB/LSB-first switchable)
3-wire serial I/O mode with automatic data transmit/receive function	–	○ (MSB/LSB-first switchable)
SBI (Serial Bus Interface) mode	○ (MSB-first)	–
2-wire serial I/O mode	○ (MSB-first)	–

Figure 5-9. Serial Interface Channel 0 Block Diagram

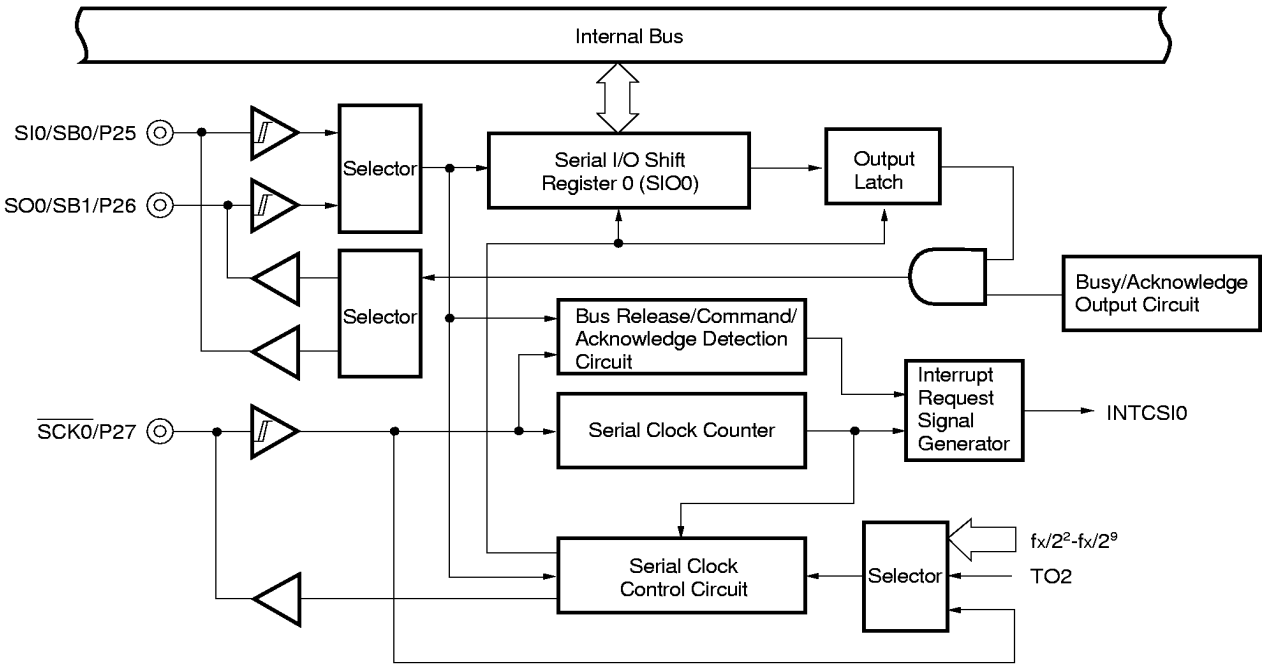
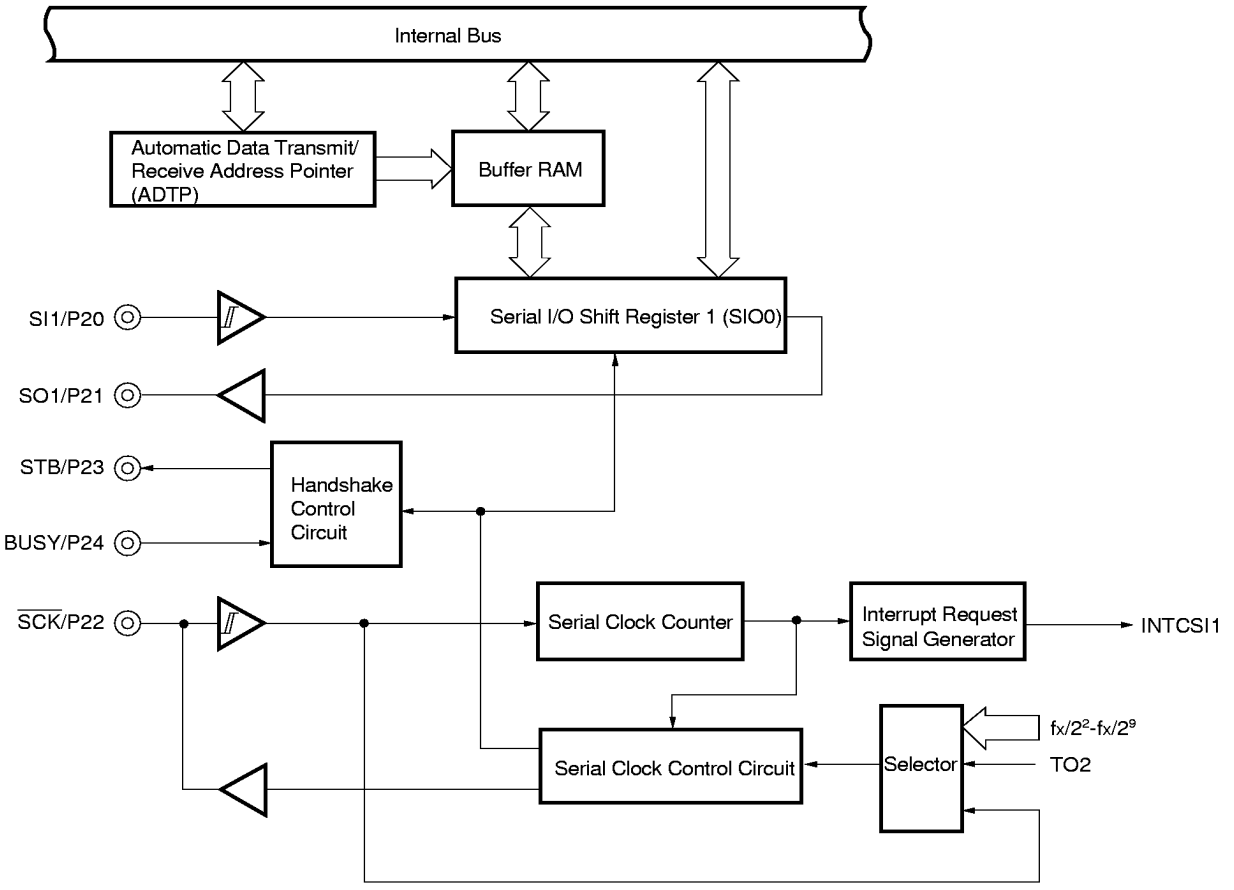


Figure 5-10. Serial Interface Channel 1 Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are the 14 interrupt sources of 3 different kind as shown below.

- Non-maskable : 1
- Maskable : 12
- Software : 1

Table 6-1. Interrupt Source List

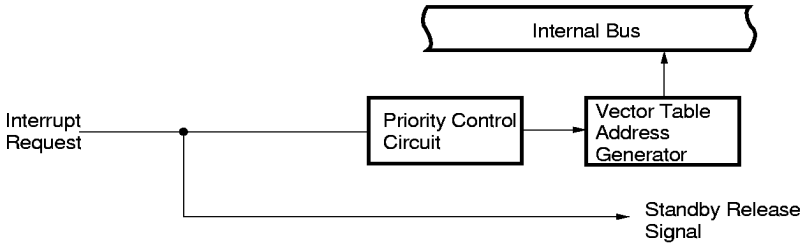
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTCSI0	Serial interface channel 0 transfer end	Internal	000EH	(B)
	6	INTCSI1	Serial interface channel 1 transfer end		0010H	
	7	INTTM3	Reference time interval signal from watch timer		0012H	
	8	INTTM0	16 bit timer/event counter match signal generation		0014H	
	9	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	10	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
	11	INTAD	A/D converter conversion end		001AH	
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. The default pririty is the priority applicable when more than one maskable interrupt request is generated. 0 is the highest priority and 11, the lowest.

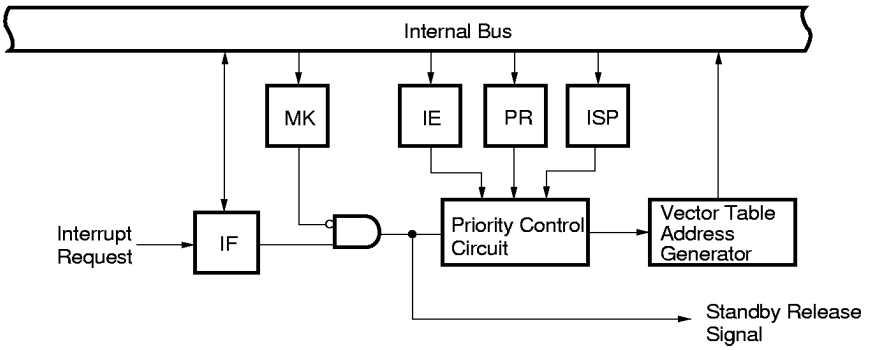
2. Basic configuration types (A) to (E) correspond to (A) to (E) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

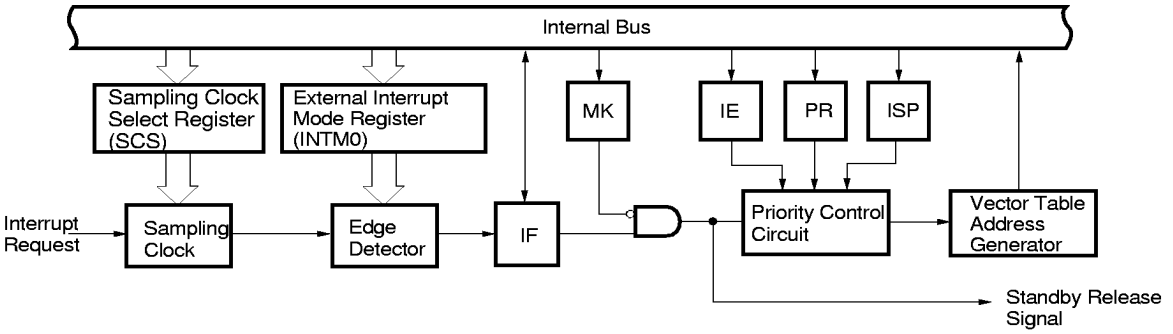
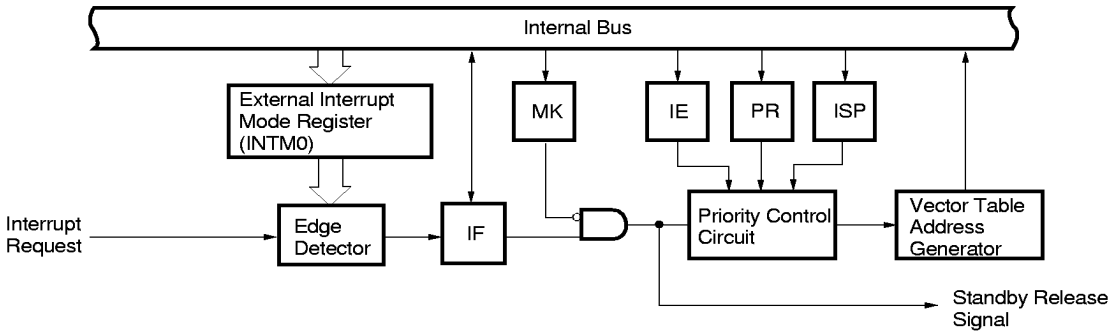
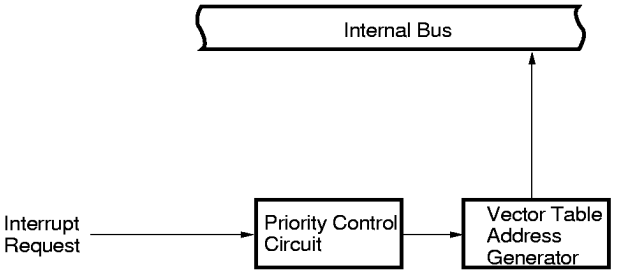


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority spcification flag

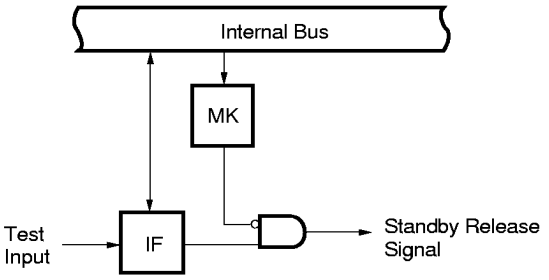
6.2 TEST FUNCTIONS

There are two test sources as shown in Table 6-2.

Table 6-2. Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

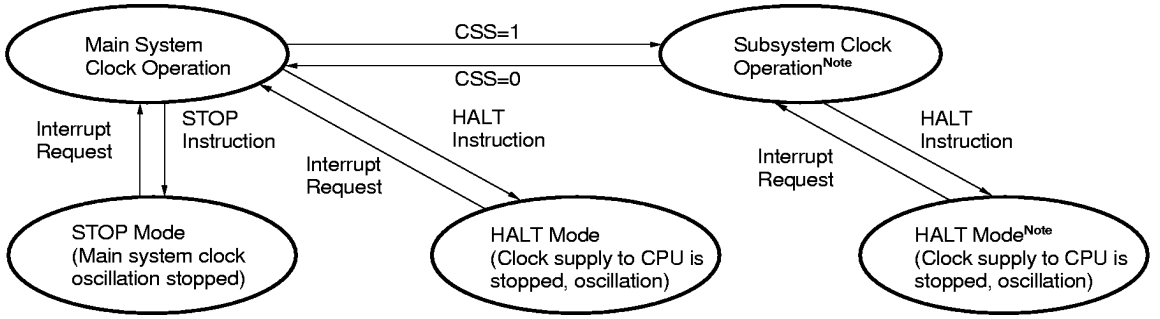
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current consumption.

- HALT mode : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operat ing mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Functions



Note The current consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

9. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer hung-up time detection.

10. INSTRUCTION SET

(1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
★ B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-Bit Instruction

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL.

(3) Bit Manipulation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call Instruction/Branch Instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT,BF, BTCLR, DBNZ

(5) Other Instruction

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (1/26)**

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P04, P10-P17, P20-P27, P30-P37, P40-P47 P50-P57, P64-P67, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	Open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P10-P17, P20-P27, P30-P37 total		–15	mA
		P01-P03, P40-P47, P50-P57, P60-P67 total		–15	mA
Output current low	I_{OL} **Note**	1 pin	Peak value	30	mA
			rms	15	mA
		P40-P47, P50-P55 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P56, P57, P60-P67 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P64-P67 total	Peak value	50	mA
			rms	20	mA
		P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note rms should be calculated as follows: [rms] = [peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

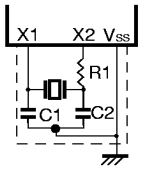
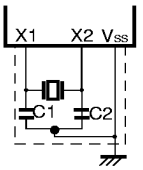
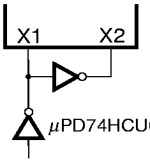
● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (2/26)**

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67			15	pF
			P60-P63			20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X) **Note 1**	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		5	
		Oscillation stabilization time **Note 2**	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f_X) **Note 1**	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		5	
		Oscillation stabilization time **Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) **Note 1**		1.0		10.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		45		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

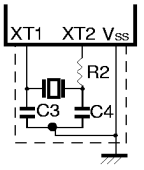
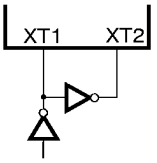
Cautions 1. When using the main system clock oscillator, wirinin the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (3/26)**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Particular care is therefore required with the wiring method when the subsystem clock is used.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (4/26)**

Recommended Oscillation Circuit Constant

Recommended oscillation circuit constant differs depending on the model.

(1) μPD78011F(A), 78012F(A), 78013F(A), 78014F(A)

(a) Main system clock: ceramic resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp.	CCR4.0MC3	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	FCR4.0MC5	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CCR4.19MC3	4.19	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	FCR4.19MC5	4.19	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CCR5.00MC3	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	FCR5.00MC5	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CCR8.00MC	8.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, surface-mount type
	FCR8.00MC5	8.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CCR8.38MC	8.38	Built-in	Built-in	2.7	5.5	Capacitor on chip, surface-mount type
	FCR8.38MC5	8.38	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CCR10.00MC	10.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, surface-mount type
	FCR10.00MC5	10.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
Murata Mfg. Co. Ltd.	CSA4.00MG	4.00	30	30	1.8	5.5	Insertion type
	CST4.00MGW	4.00	Built-in	Bkuilt-in	1.8	5.5	Capacitor on chip, insertion type
	CSA4.19MG	4.19	30	30	1.8	5.5	Insertion type
	CST4.19MGW	4.19	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CSA5.00MG	5.00	30	30	1.8	5.5	Insertion type
	CST5.00MGW	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	CSA8.00MTZ	8.00	30	30	2.7	5.5	Insertion type
	CST8.00MTW	8.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CSA8.38MTZ	8.38	30	30	2.7	5.5	Insertion type
	CST8.38MTW	8.38	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type
	CSA10.00MTZ	10.00	30	30	2.7	5.5	Insertion type
	CST10.00MTW	10.00	Built-in	Built-in	2.7	5.5	Capacitor on chip, insertion type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (5/26)

(b) Main system clock: ceramic resonator (T_A = –20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kyocera Corp.	PBRC4.00A	4.00	33	33	1.8	5.5	Surface-mount type
	RBRC4.00B	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-4.00MSA	4.00	33	33	1.8	5.5	Insertion type
	KBR-4.00MKS	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	PBRC5.00A	5.00	33	33	1.8	5.5	Surface-mount type
	RBRC5.00B	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-5.00MSA	5.00	33	33	1.8	5.5	Insertion type
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	KBR-8M	8.00	33	33	2.7	5.5	Insertion type
	KBR-10M	10.00	33	33	2.7	5.5	Insertion type

(2) μPD78015F(A), 78016F(A)

(a) Main system clock: ceramic resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant			Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co. Ltd.	CSB1000J	1.00	100	100	5.6	1.8	5.5	Insertion type
	CSA2.00MG040	2.00	100	100	0	1.8	5.5	Insertion type
	CST2.00MG040		Built-in	Built-in	0	1.8	5.5	Capacitor on chip, insertion type
	CSA4.00MG040	4.00	100	100	0	1.8	5.5	Insertion type
	CST4.00MGW040		Built-in	Built-in	0	1.8	5.5	Capacitor on chip, insertion type
	CSA6.00MG	6.00	30	30	0	1.8	5.5	Insertion type
	CST6.00MGW		Built-in	Built-in	0	1.8	5.5	Capatitor on chip, insertion type
	CSA10.0MTZ	10.0	30	30	0	1.8	5.5	Insertion type
	CST10.0MTW		Built-in	Built-in	0	1.8	5.5	Capatitor on chip, insertion type
TDK	FCR4.0MC5	4.0	Built-in	Built-in	2.2	1.8	5.5	Capatitor on chip, insertion type
	FCR10.0MC	10.0	Built-in	Built-in	1.0	1.8	5.5	Capatitor on chip, insertion type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (6/26)**

(b) Main system clock: ceramic resonator (T_A = –20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kyocera Corp.	PBRC4.00A	4.00	33	33	1.8	5.5	Surface-mount type
	RBRC4.00B	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-4.00MSA	4.00	33	33	1.8	5.5	Insertion type
	KBR-4.00MKS	4.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	PBRC5.00A	5.00	33	33	1.8	5.5	Surface-mount type
	RBRC5.00B	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, surface-mount type
	KBR-5.00MSA	5.00	33	33	1.8	5.5	Insertion type
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5	Capacitor on chip, insertion type
	KBR-8M	8.00	33	33	2.7	5.5	Insertion type
	KBR-10M	10.00	33	33	2.7	5.5	Insertion type

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (7/26)**

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open drain)	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		15	V
				0.8 V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V **Note**	0.9 V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60-P63	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P04, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V **Note**	0		0.1 V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50-P57, P60-P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P20-P27 P30-P37, P40-P47, P64-P67	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain, pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When using XT1/P04 as P04, input the inverse of P04 to XT2 using an inverter.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (8/26)**

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakege current low	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			–20	μA
	I_{LIL3}		P60-P63			–3 Note	μA
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60-P63		20	40	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67		15	40	90	kΩ

Note For P60-P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of –200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is –3 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (9/26)**

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	10.00 MHz crystal oscillation operation mode	V_{DD} = 5.0 V ± 10 % Note 2		9.0	18.0	mA
			V_{DD} = 3.0 V ± 10 % Note 3		1.3	2.6	mA
	I_{DD2}	10.00 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 % Note 2		2.4	4.8	mA
			V_{DD} = 3.0 V ± 10 % Note 3		1.2	2.4	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode Note 4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		35	70	μA
			V_{DD} = 2.0 V ± 10 %		24	48	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ± 10 %		25	50	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.0 V ± 10 %		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode when using feedback resistor	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.0 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode when not using feedback resistor	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.0 V ± 10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the built-in pull-up resistor.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when the PCC is set to 04H)

4. When main system clock stopped.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (10/26)**

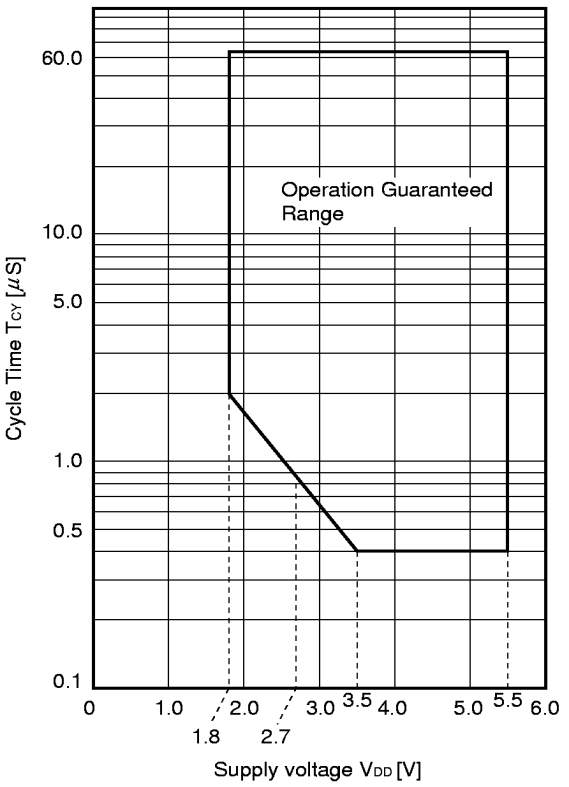
AC Characteristics

(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		64	μs
			2.7 V ≤ V_{DD} < 3.5 V	0.8		64	μs
			1.8 V ≤ V_{DD} < 2.7 V	2.0		64	μs
		Operating on subsystem clock		40	122	125	μs
TI0 input frequency	t_{TIH0} t_{TIL0}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$+0.2 Note			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t_{TIH1} t_{TIL1}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high/low-level width	t_{INTH} t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$+0.1 Note			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$+0.2 Note			μs
			1.8 V ≤ V_{DD} < 2.7 V	$2/f_{sam}$+0.5 Note			μs
		INTP1-INTP3, KR0-KR7	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_X/2^{N+1}$, f_X/64 and f_X/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (11/26)**

(2) Read/Write Operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}$–30		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.5+2n)t_{CY}$–50	ns
	t_{ADD2}			$(3+2n)t_{CY}$–100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(1+2n)t_{CY}$–25	ns
	t_{RDD2}			$(2.5+2n)t_{CY}$–100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}$–20		ns
	t_{RDL2}		$(2.5+2n)\ t_{CY}$–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			$0.5t_{CY}$	ns
	t_{RDWT2}			$1.5t_{CY}$	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			$0.5t_{CY}$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$+10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}	Load resistor ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.5+2n)\ t_{CY}$ –20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		$0.5t_{CY}$–30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$1.5t_{CY}$–30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}–10	t_{CY}+40	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 4.5 to 5.5 V	$0.5t_{CY}$+5	$0.5t_{CY}$+30	ns
			$0.5t_{CY}$+15	$0.5t_{CY}$+90	ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 4.5 to 5.5 V	5	30	ns
			15	90	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 4.5 to 5.5 V	t_{CY}	t_{CY}+60	ns
			t_{CY}	t_{CY}+100	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$+80	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$+80	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (12/26)

(3) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
	t_{KL1}		t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{SCK0}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
	t_{KL2}	2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK0}$ rise, fall time	t_{R2} t_{F2}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (13/26)**

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2–50			ns
	t_{KL3}			t_{KCY3}/2–150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF **Note**	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the SB0, SB1 and $\overline{SCK0}$ output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (14/26)**

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH4} t_{KL4}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.0 V ≤ V_{DD} < 4.5 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF **Note**	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (15/26)**

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
			2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	t_{KCY5}/2–160			ns
				t_{KCY5}/2–190			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5}/2–50			ns
				t_{KCY5}/2–100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (16/26)**

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH6}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL6}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF **Note**	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		800	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (17/26)**

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
	t_{KL7}		t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
	t_{KL8}	2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}			400			ns
SO0 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R8}	When external device expansion function is used				160	ns
	t_{F8}	When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO1 output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (18/26)**

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2–50			ns
	t_{KL9}		t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF **Note**			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	4.5 V ≤ V_{DD} ≤ 5.5 V	t_{KCY9}–30		t_{KCY9}+30	ns
		2.0 V ≤ V_{DD} < 2.7 V	t_{KCY9}–60		t_{KCY9}+60	ns
			t_{KCY9}–90		t_{KCY9}+90	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				2t_{KCY9}	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (19/26)**

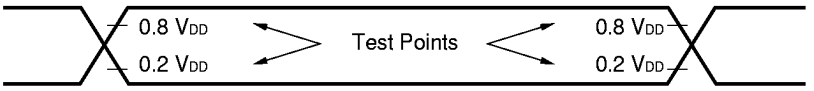
(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When external device expansion function is used				160	ns
		When external device expansion function is not used				1000	ns

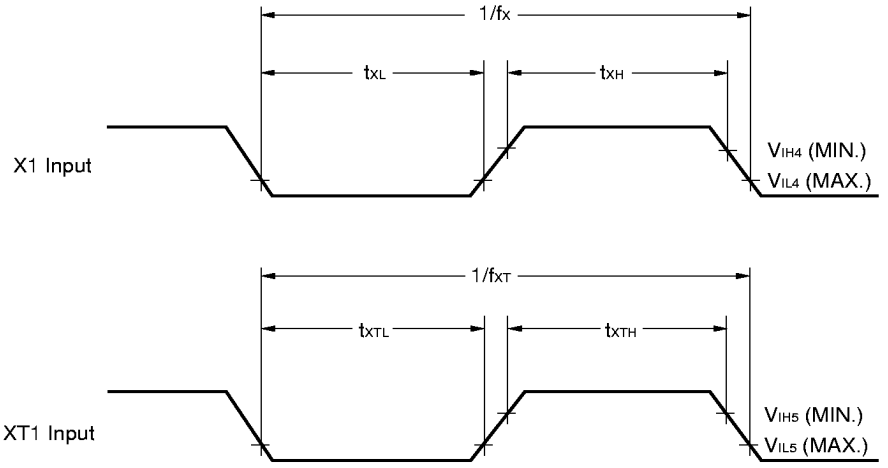
Note C is the load capacitance of the SO1 output line.

● Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (20/26)

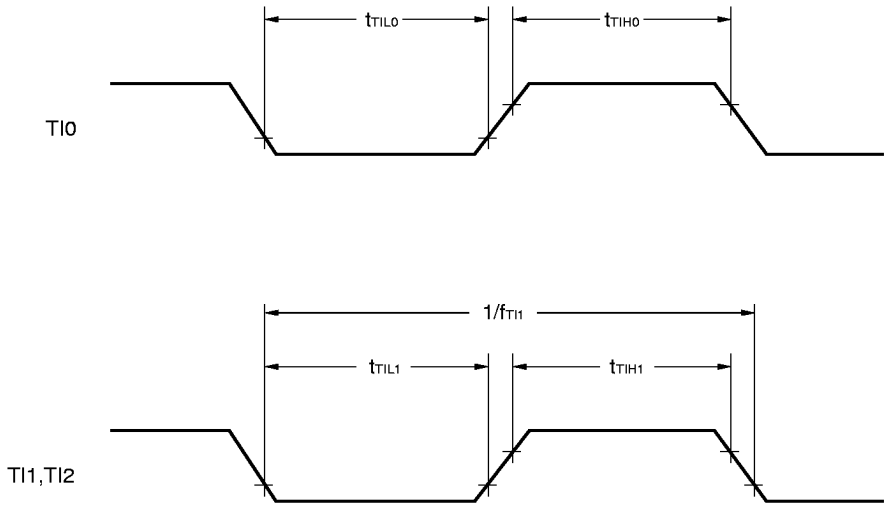
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing



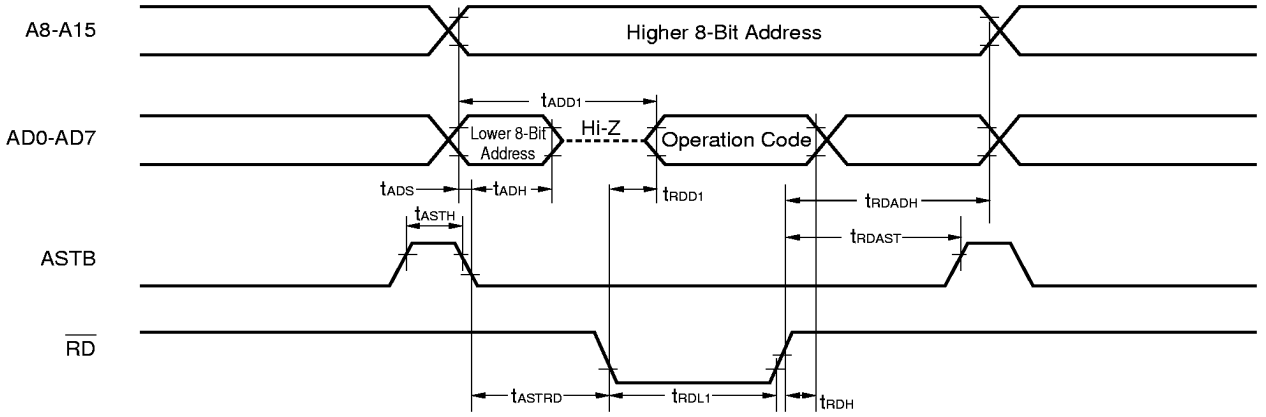
TI Timing



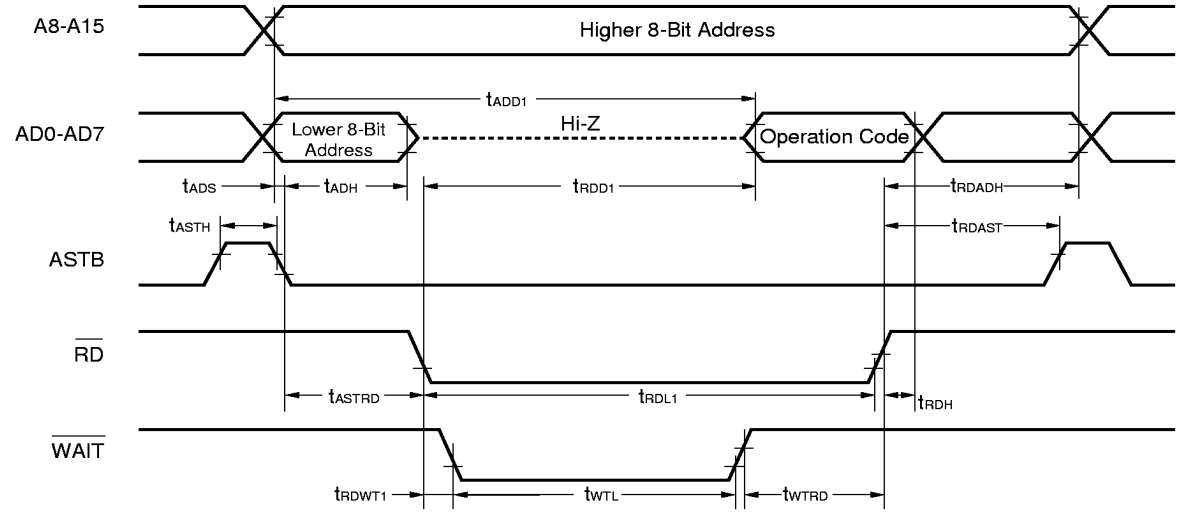
● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (21/26)**

Read/Write Operation

External fetch (No wait):

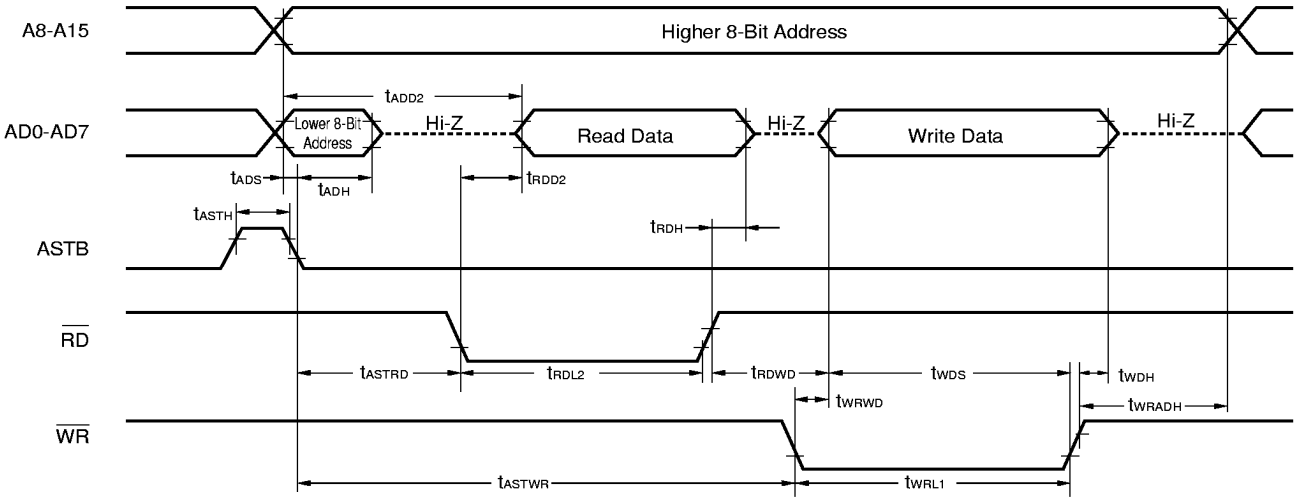


External fetch (Wait insertion):

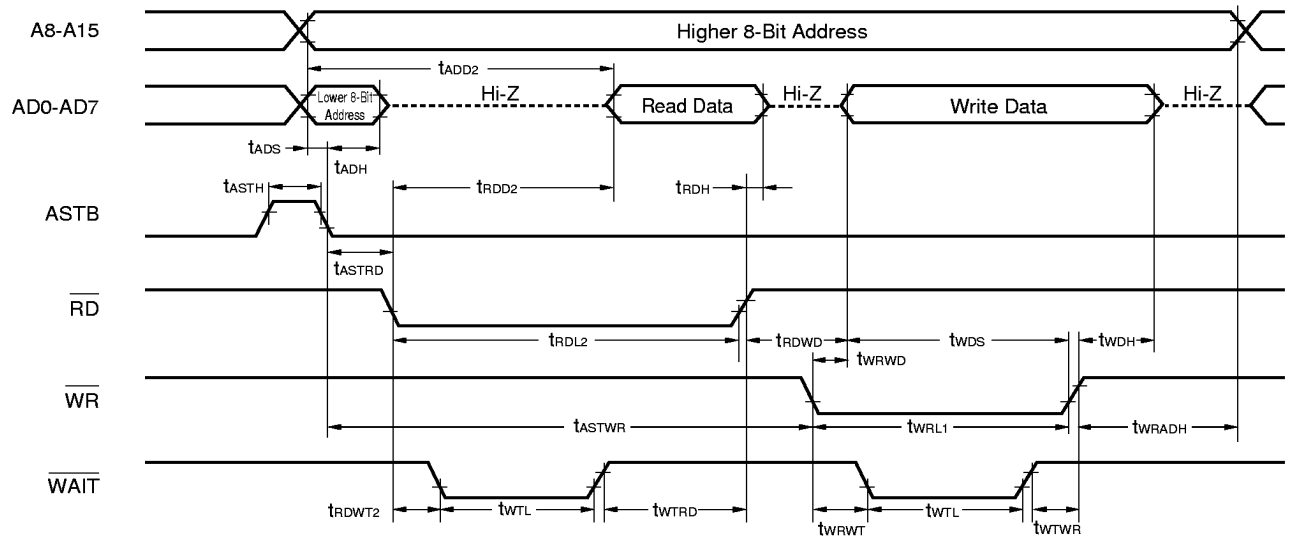


● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (22/26)**

External data access (No wait):



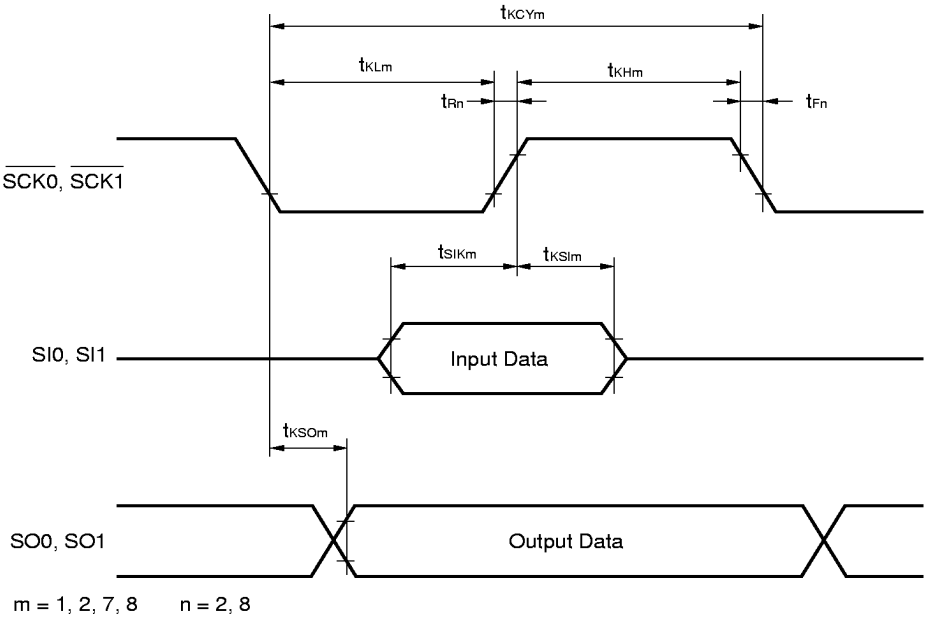
External data access (Wait insertion):



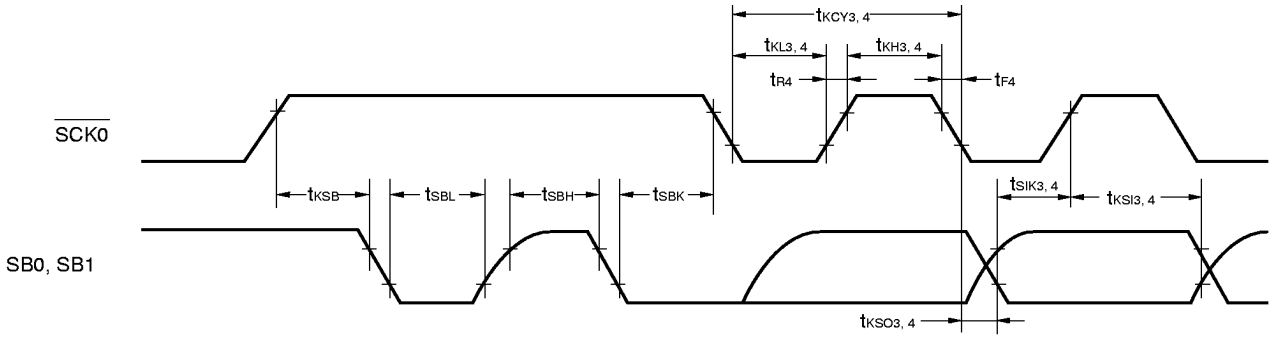
● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (23/26)**

Serial Transfer Timing

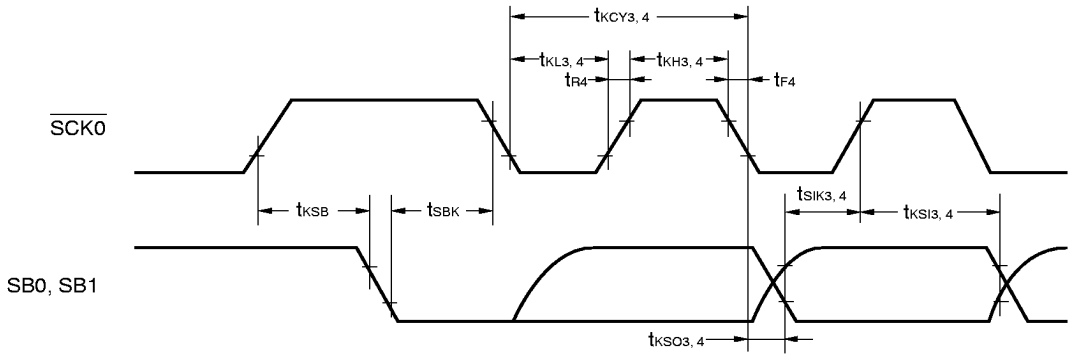
3-wire serial I/O mode:



SBI mode (Bus release signal transfer):

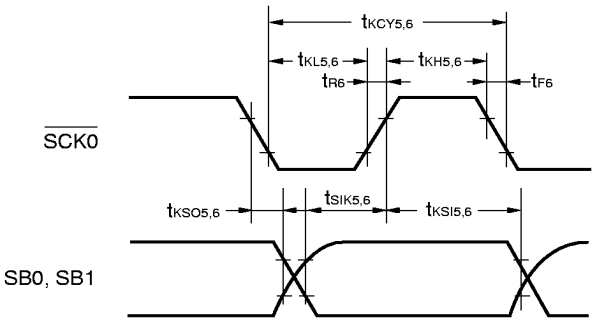


SBI Mode (command signal transfer):

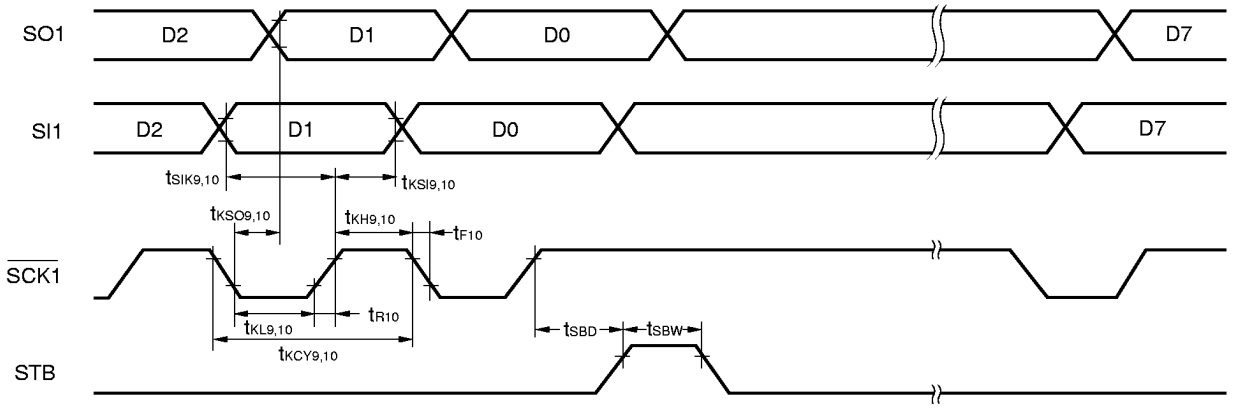


● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (24/26)**

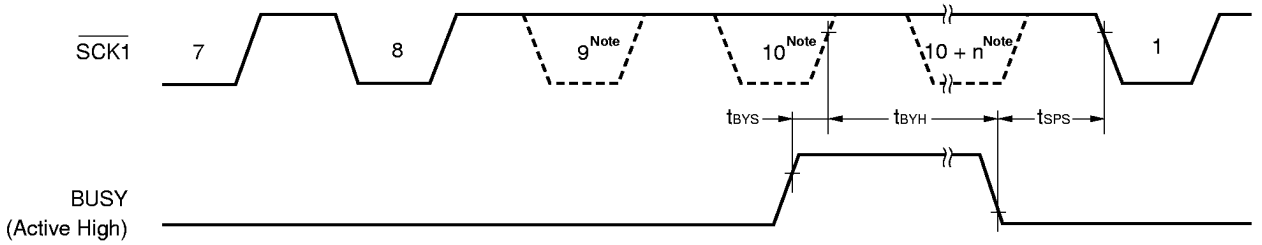
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (25/26)**

A/D converter characteristics (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error **Note**		2.7 V ≤ AV_{REF} ≤ AV_{DD}			0.6	%
		1.8 V ≤ AV_{REF} ≤ 2.7 V			1.4	%
Conversion time	t_{CONV}	2.0 V ≤ AV_{DD} < 5.5 V	19.1		200	μs
		1.8 V ≤ AV_{DD} < 2.0 V	38.2		200	μs
Sampling time	t_{SAMP}		24/fx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		4	14		kΩ

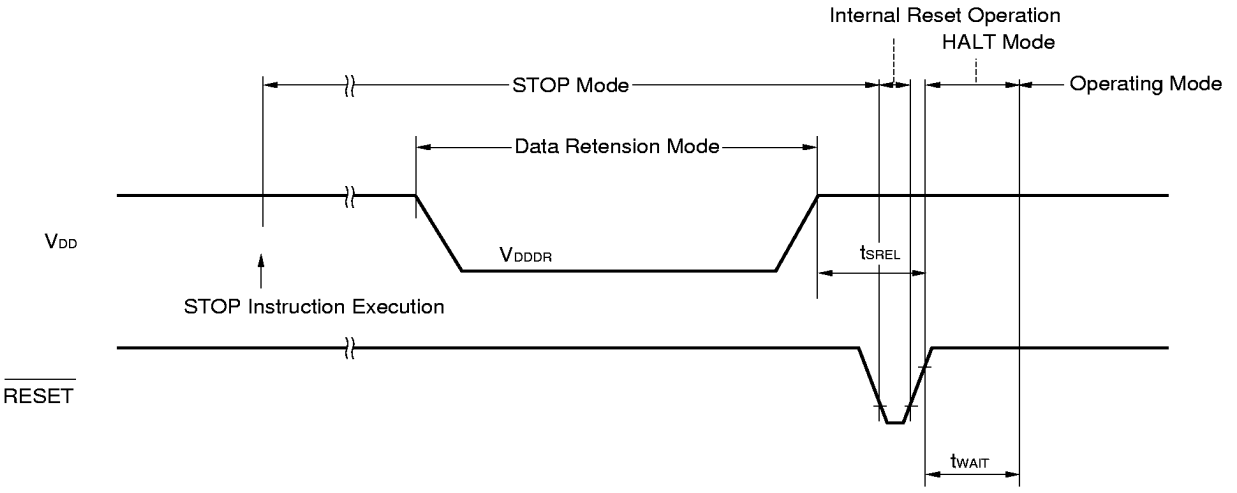
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resister disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{18}/fx		ms
		Release by interrupt request		**Note**		ms

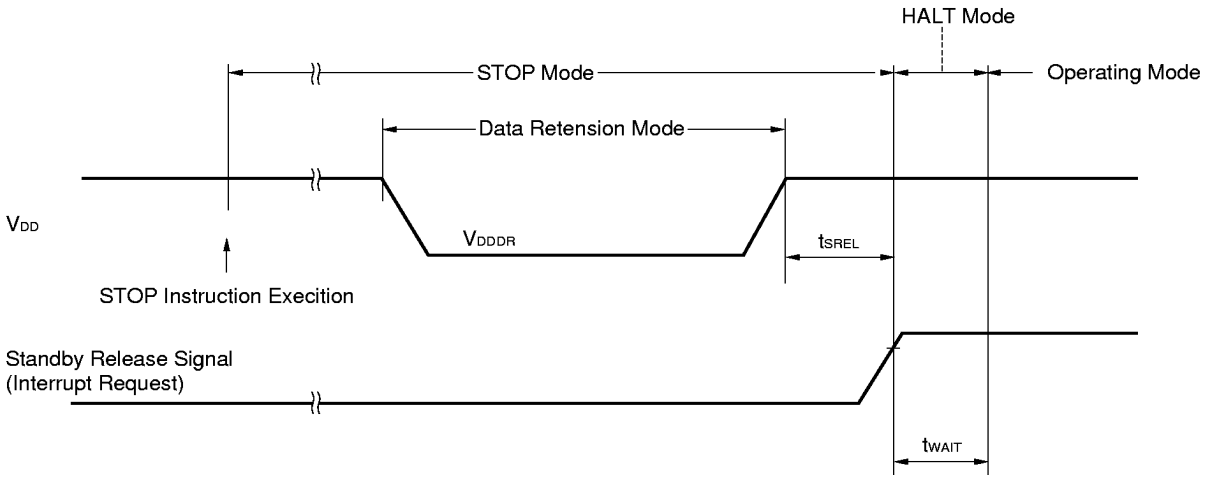
Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2^{13}/fx and 2^{15}/fx to 2^{18}/fx is possible.

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)

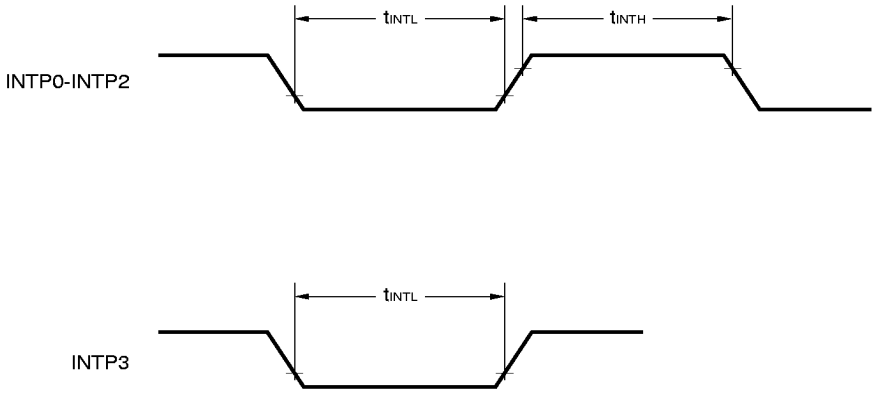


● **Electrical Specifications of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) (26/26)**

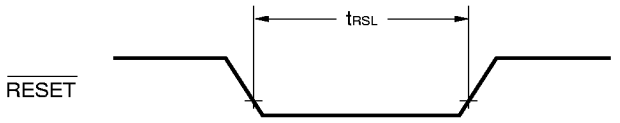
Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



★ ● **Electrical Specifications of μPD78012F(A2) (1/20)**

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P04, P10-P17, P20-P27, P30-P37, P40-P47 P50-P57, P64-P67, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	Open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P10-P17, P20-P27, P30-P37 total		–15	mA
		P01-P03, P40-P47, P50-P57, P60-P67 total		–15	mA
Output current low	I_{OL} **Note**	1 pin	Peak value	30	mA
			rms	15	mA
		P40-P47, P50-P55 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P56, P57, P60-P67 total	Peak value	100	mA
			rms	70	mA
		P01-P03, P64-P67 total	Peak value	50	mA
			rms	20	mA
		P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	T_A			–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note rms should be calculated as follows: [rms] = [peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78012F(A2) (2/20)**

Permissible Injection Current characteristics at overvoltage application (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Positive direction injection current ($V_{IN} > V_{DD}$)	I_{IJH1}	1 pin	Input port other than ANIn (n = 0-7)	Peak value			2	mA
				Average value			0.2	mA
	I_{IJH2}		ANIn (n = 0-7)	Peak value			0.2	mA
				Average value			0.02	mA
	I_{IJH3}	Total for all input pins		Peak value			16	mA
				Average value			1.6	mA
	I_{IJH4}	Total for ANIn (n = 0-7)		Peak value			0.2	mA
				Average value			0.02	mA
Negative direction injection current ($V_{IN} < V_{SS}$)	I_{IJL1}	1 pin	Input port other than ANIn (n = 0-7)	Peak value			–0.1	mA
				Average value			–0.01	mA
	I_{IJL2}		ANIn (n = 0-7)	Peak value			–0.3	mA
				Average value			–0.03	mA
	I_{IJL3}	Total for all input pins		Peak value			–0.8	mA
				Average value			–0.08	mA
	I_{IJL4}	Total for ANIn (n = 0-7)		Peak value			–0.3	mA
				Average value			–0.03	mA

Cautions
1. **When injection current flows through an analog input pin (ANIn : n = 0-7), the A/D conversion result of the analog input becomes the rated value when there is no injection current ±2LSB.**
2. **When injection current flows through several analog input pins (ANIn : n = 0-7), the A/D conversion result of the analog input becomes the rated value when there is no injection current ±4LSB.**
3. **The average value (absolute value) of the pin injection current is obtained by the following formula.**

$$\text{Average value} = \left((1/T)\int_0^T |\, i(t)\,|^{3/2}dt\right)^{3/2}$$

where, i(t) indicates the pin injection current. The maximum value of | i(t) | is the peak value.

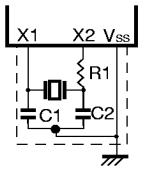
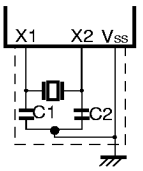
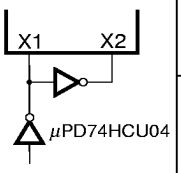
Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67			15	pF
			P60-P63			20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78012F(A2) (3/20)**

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X) **Note 1**		1		8	MHz
		Oscillation stabilization time **Note 2**	After V_{DD} reaches oscillator voltage range MIN.			10	ms
Crystal resonator		Oscillator frequency (f_X) **Note 1**		1		8	MHz
		Oscillation stabilization time **Note 2**				10	ms
External clock		X1 input frequency (f_X) **Note 1**		1.0		8.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		55		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

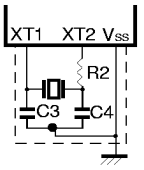
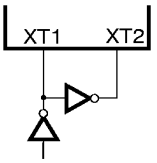
Cautions 1. When using the main system clock oscillator, wirinin the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

● **Electrical Specifications of μPD78012F(A2) (4/20)**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2			1.2	2	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Particular care is therefore required with the wiring method when the subsystem clock is used.

● **Electrical Specifications of μPD78012F(A2) (5/20)**

DC Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10%)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$		0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open drain)		0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2		0.8 V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67		0		0.3 V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$		0		0.18 V_{DD}	V
	V_{IL3}	P60-P63 (N-ch open drain)		0		0.3 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2		0		0.2 V_{DD}	V
Output voltage high	V_{OH1}	I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50-P57, P60-P63	I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P20-P27 P30-P37, P40-P47, P64-P67	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	N-ch open-drain, pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, $\overline{\text{RESET}}$			10	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakege current low	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, $\overline{\text{RESET}}$			–10	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			–20	μA
	I_{LIL3}		P60-P63			–10 **Note**	μA

Note For P60-P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of –200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is –10 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78012F(A2) (6/20)**

DC Characteristics (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Output leakage current high	I_{LOH}	V_{OUT} = V_{DD}			10	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V			–10	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60-P63	20	40	120	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P03, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67	15	40	120	kΩ
Supply current Note 1	I_{DD1}	8.00 MHz crystal oscillation operation mode Note 2		9.0	29.0	mA
	I_{DD2}	8.00 MHz crystal oscillation HALT mode Note 2		2.4	6.5	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode Note 3		60	1200	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 3		25	1000	μA
	I_{DD5}	XT1 = V_{DD} STOP mode when using feedback resistor		1	1000	μA
	I_{DD6}	XT1 = V_{DD} STOP mode when not using feedback resistor		0.1	1000	μA

Notes 1. The current which flows in the V_{DD} pin and AV_{DD} pin. However, it does not include the current flowing in the A/D converter and built-in pull-up resistor.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When main system clock stopped.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

● **Electrical Specifications of μPD78012F(A2) (7/20)**

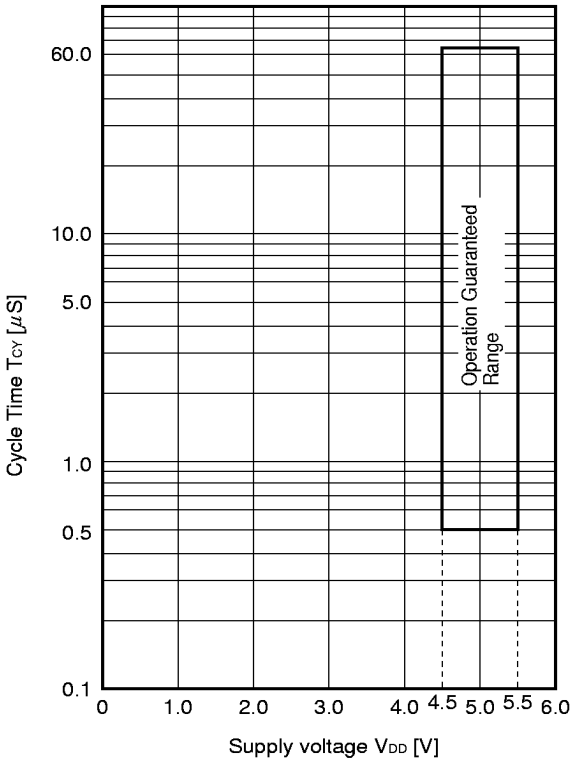
AC Characteristics

(1) Basic Operation (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	0.5		64	μs
		Operating on subsystem clock	40	122	125	μs
TI0 input high/low-level width	t_{TIH0} t_{TIL0}		$2/f_{sam}$+0.1 **Note**			μs
TI1, TI2 input frequency	f_{TI1}		0		2	kHz
TI1, TI2 input high/low-level width	t_{TIH1} t_{TIL1}		200			μs
Interrupt request input high/low-level width	t_{INTH} t_{INTL}	INTP0	$2/f_{sam}$+0.1 **Note**			μs
		INTP1-INTP3, KR0-KR7	10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}		10			μs

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_x/2^{N+1}$, f_x/64 and f_x/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



● **Electrical Specifications of μPD78012F(A2) (8/20)**

(2) Read/Write Operation (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}$–30		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.5+2n)t_{CY}$–50	ns
	t_{ADD2}			$(3+2n)t_{CY}$–100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(1+2n)t_{CY}$–25	ns
	t_{RDD2}			$(2.5+2n)t_{CY}$–100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}$–20		ns
	t_{RDL2}		$(2.5+2n)$ t_{CY}–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			$0.5t_{CY}$	ns
	t_{RDWT2}			$1.5t_{CY}$	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			$0.5t_{CY}$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$+10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}	Load resistor ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.5+2n)$ t_{CY} –20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		$0.5t_{CY}$–30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$1.5t_{CY}$–30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}–10	t_{CY}+40	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		$0.5t_{CY}$+5	$0.5t_{CY}$+30	ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		5	6	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		t_{CY}	t_{CY}+60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$+80	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$+80	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

● **Electrical Specifications of μPD78012F(A2) (9/20)**

(3) Serial Interface (T_A = –40 to +125 °C, V_{DD} = 5 V ± 10 %)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}		1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2-100$			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}		150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		500			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			400	ns

Note C is the load capacitance of $\overline{SCK0}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}			1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH2} t_{KL2}			500			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}			150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			500			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**				400	ns
$\overline{SCK0}$ rise, fall time	t_{R2} t_{F2}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

● **Electrical Specifications of μPD78012F(A2) (10/20)**

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}		1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}		150			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}		$t_{KCY3}/2$			ns
SB0, SB1output delay time from $\overline{SCK0}\downarrow$	t_{KSO3}	R = 1 kΩ, C = 100 pF **Note**			300	ns
SB0, SB1↓ from $\overline{SCK0}\downarrow$	t_{KSB}		t_{KCY3}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}		t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the SB0, SB1 and $\overline{SCK0}$ output line.

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}			1000			ns
$\overline{SCK0}$ high/low-level width	t_{KH4} t_{KL4}			500			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK4}			150			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO4}	R = 1 kΩ, C = 100 pF **Note**				400	ns
SB0, SB1↓ from $\overline{SCK0}\downarrow$	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● **Electrical Specifications of μPD78012F(A2) (11/20)**

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}		$t_{KCY5}/2-160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		$t_{KCY5}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		350			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}		600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}				300	ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note				500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

● **Electrical Specifications of μPD78012F(A2) (12/20)**

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}		1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH7} t_{KL7}		$t_{KCY7}/2-100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK7}		150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI7}		500			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO7}	C = 100 pF **Note**			400	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}			1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH8} t_{KL8}			500			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK8}			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI8}			500			ns
SO0 output delay time from $\overline{SCK1}\downarrow$	t_{KSO8}	C = 100 pF **Note**				400	ns
$\overline{SCK1}$ rise, fall time	t_{R8} t_{F8}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO1 output line.

● **Electrical Specifications of μPD78012F(A2) (13/20)**

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}		1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH9} t_{KL9}		$t_{KCY9}/2-100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}		150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		500			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF **Note**			400	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY9}/2-100$		$t_{KCY9}/2+100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY9}/2-30$		$t_{KCY9}/2+30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}		150			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

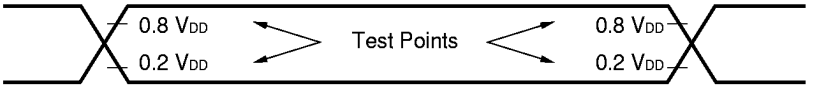
(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}			1000			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}			500			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}			150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}			500			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF **Note**				400	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{FB}	When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

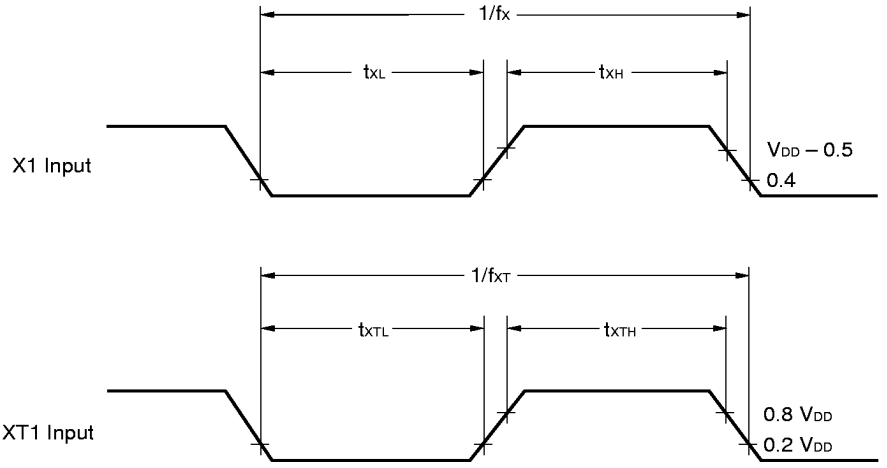
Note C is the load capacitance of the SO1 output line.

● **Electrical Specifications of μPD78012F(A2) (14/20)**

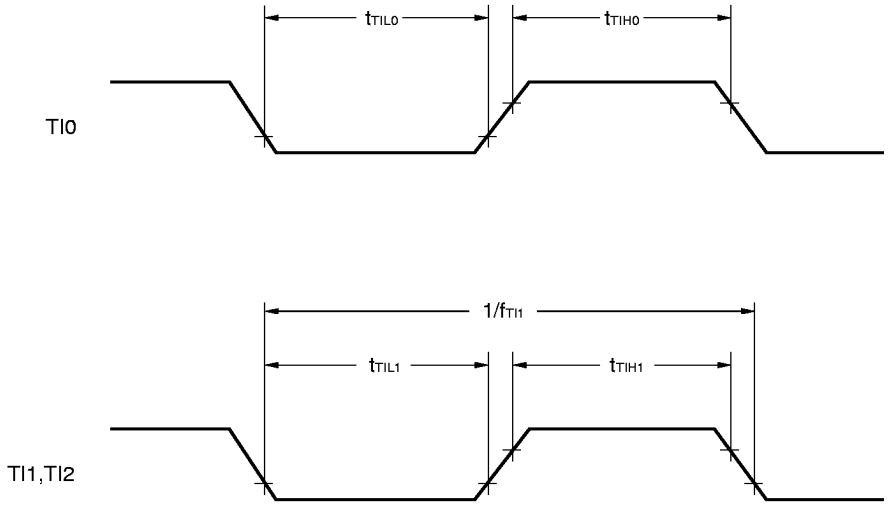
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing



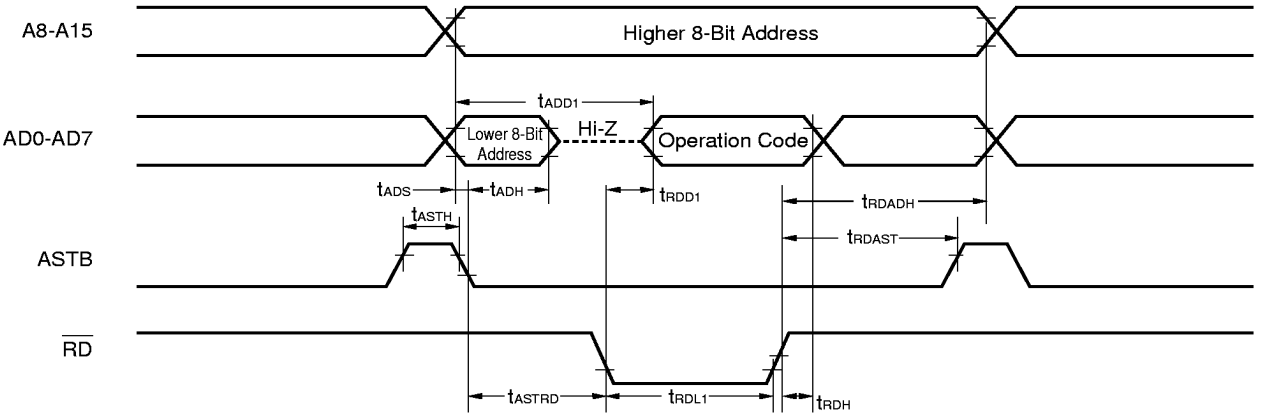
TI Timing



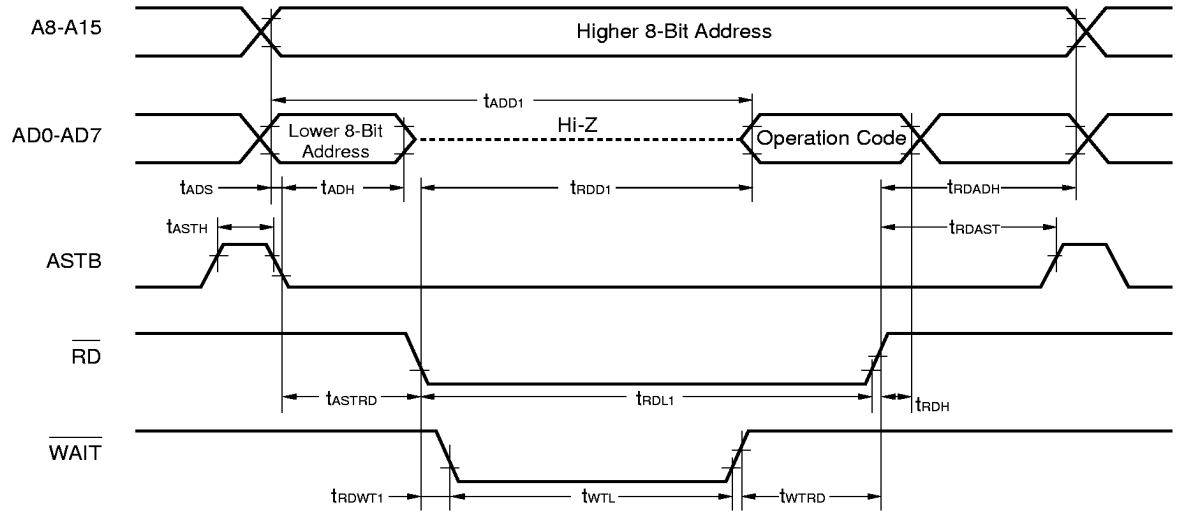
● **Electrical Specifications of μPD78012F(A2) (15/20)**

Read/Write Operation

External fetch (No wait):

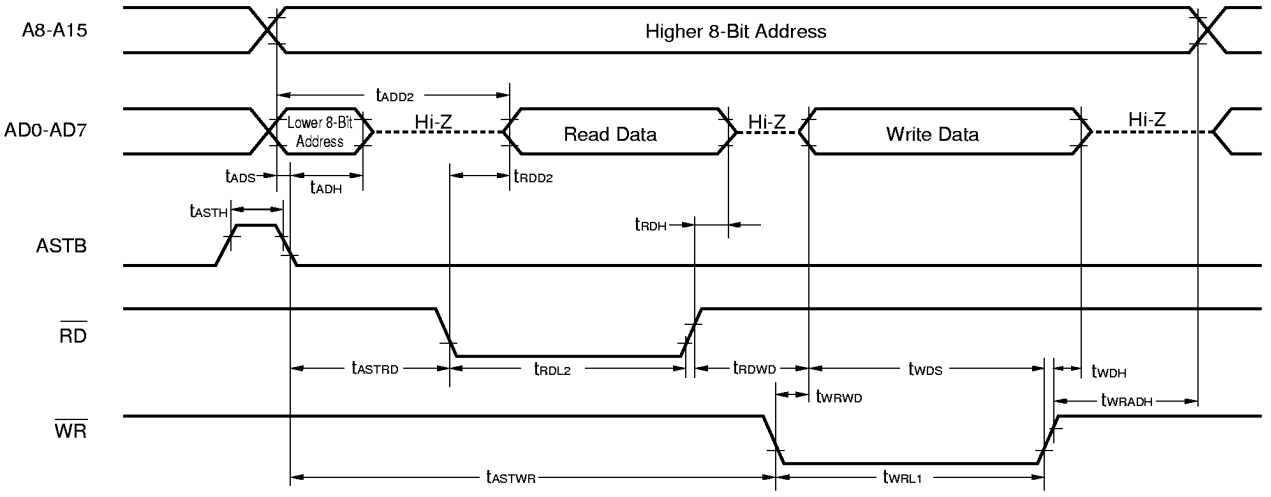


External fetch (Wait insertion):

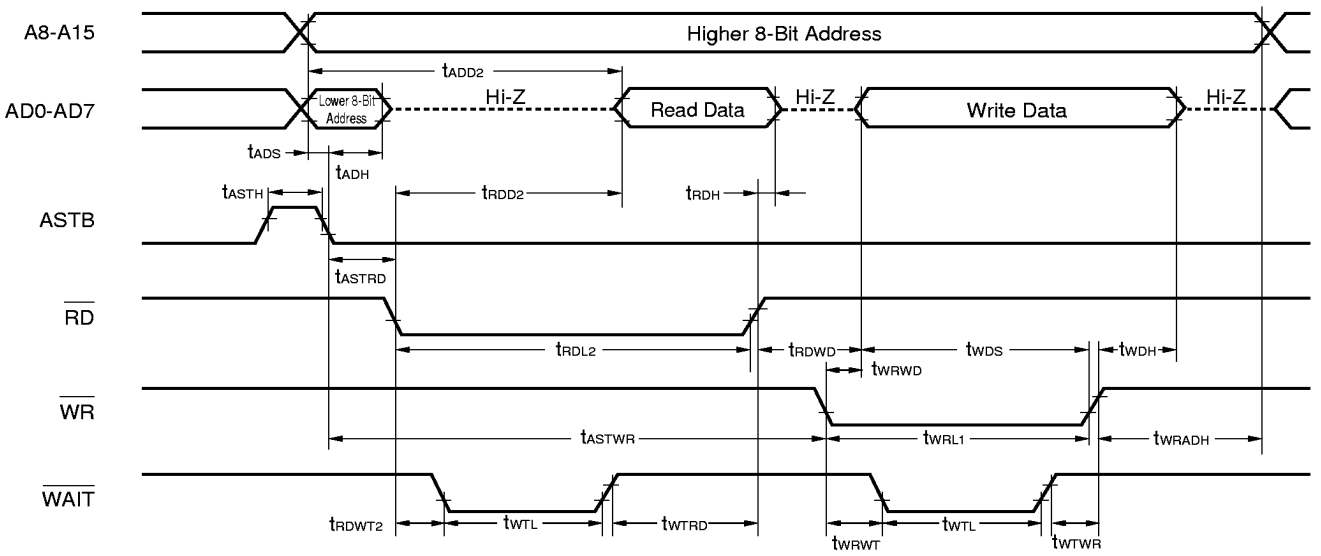


● **Electrical Specifications of μPD78012F(A2) (16/20)**

External data access (No wait):



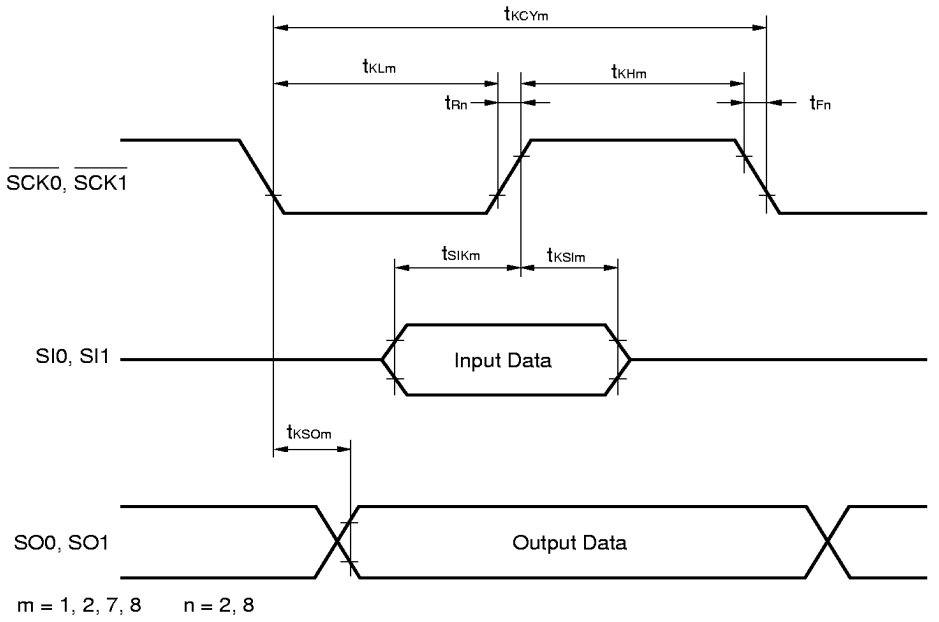
External data access (Wait insertion):



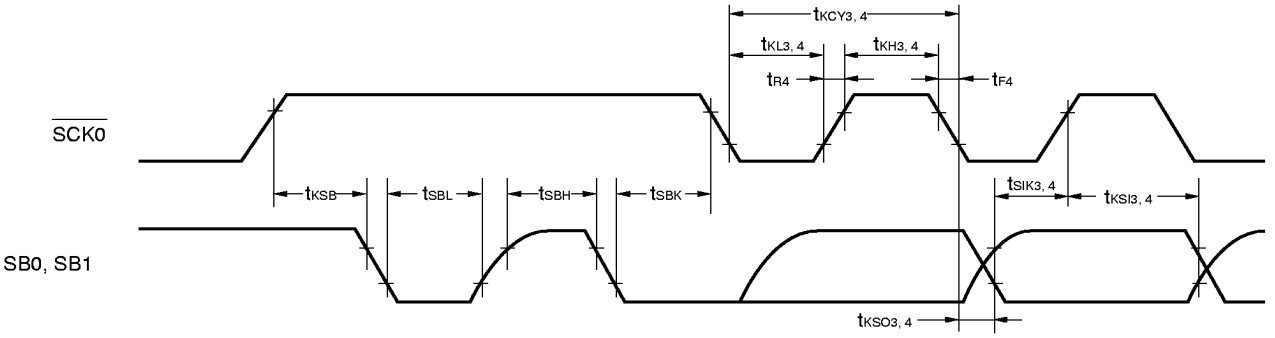
● **Electrical Specifications of μPD78012F(A2) (17/20)**

Serial Transfer Timing

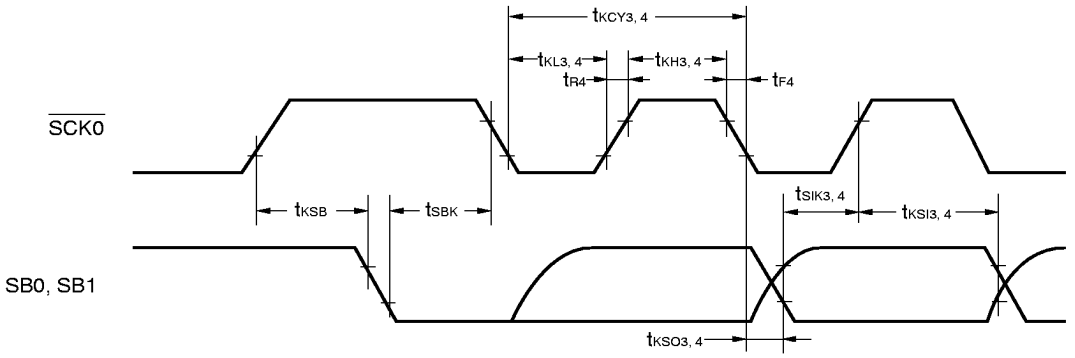
3-wire serial I/O mode:



SBI mode (Bus release signal transfer):

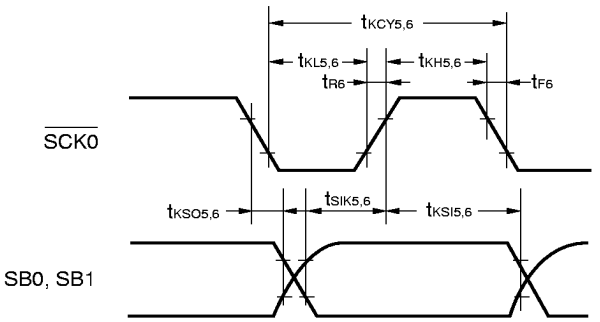


SBI Mode (command signal transfer):

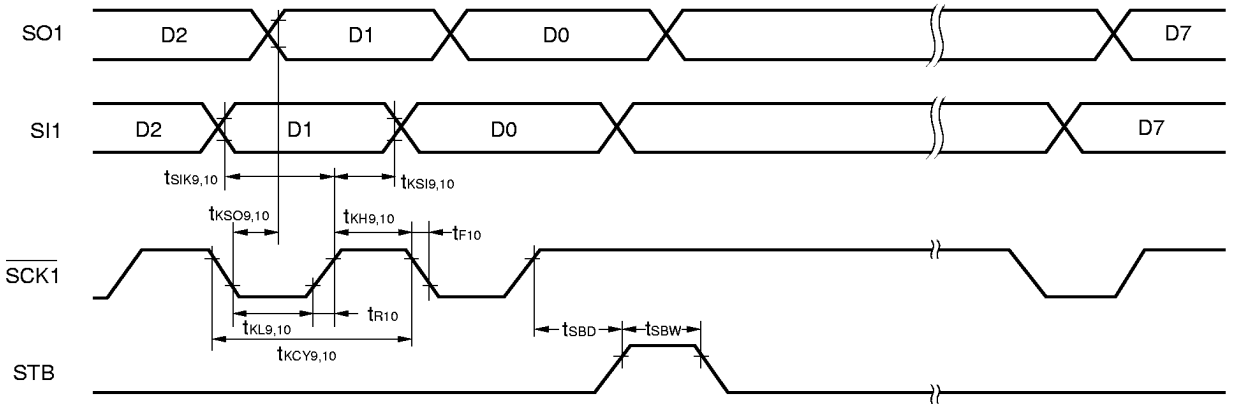


● **Electrical Specifications of μPD78012F(A2) (18/20)**

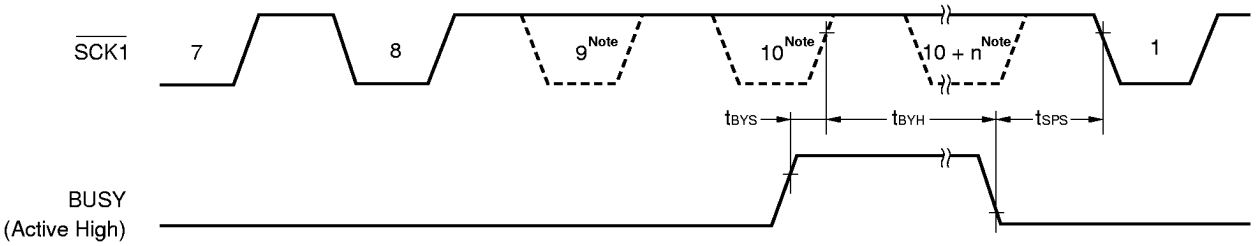
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

● **Electrical Specifications of μPD78012F(A2) (19/20)**

A/D converter characteristics (T_A = –40 to +125 °C, AV_{DD} = V_{DD} = 5.0 V ± 10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD}			1.0	%
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	23.8		200	μs
Sampling time	t_{SAMP}		24/fx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		4	14		kΩ

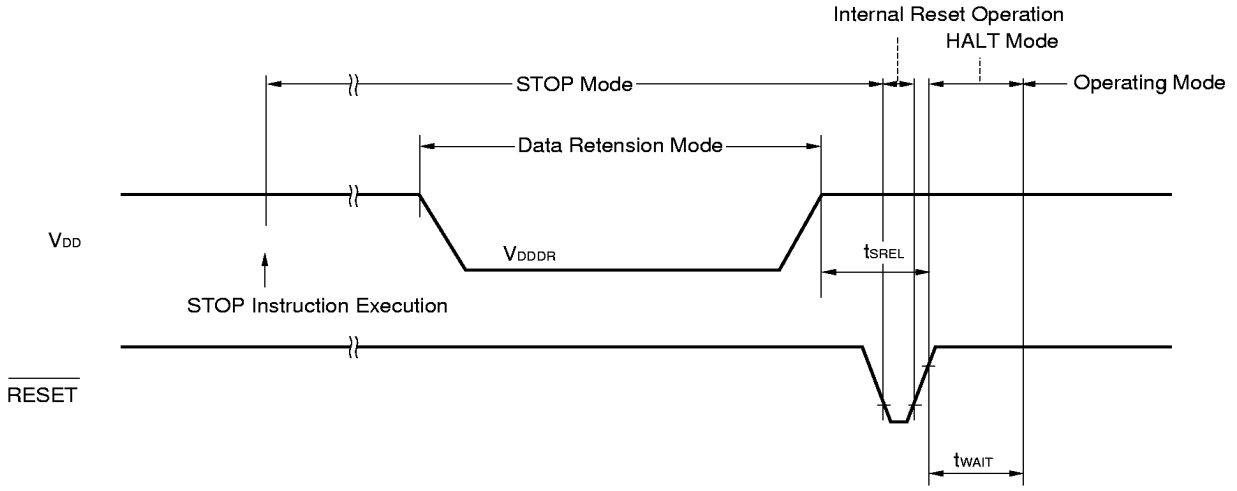
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +125 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.7		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.7 V Subsystem clock stop and feed-back resister disconnected		0.1	1000	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{18}/fx		ms
		Release by interrupt request		**Note**		ms

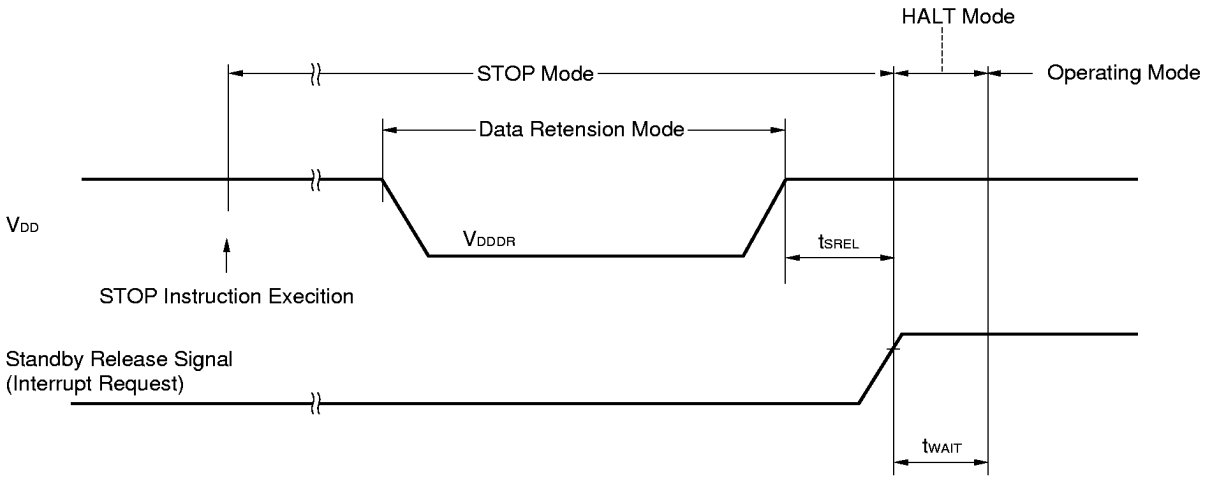
Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2^{13}/fx and 2^{15}/fx to 2^{18}/fx is possible.

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

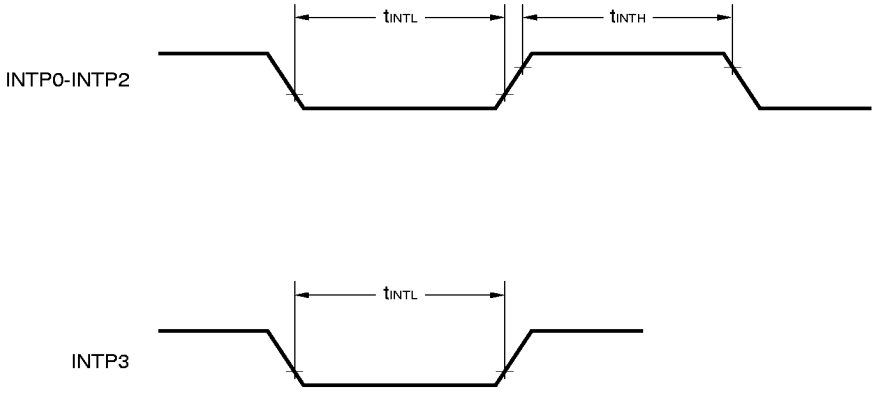


● **Electrical Specifications of μPD78012F(A2) (20/20)**

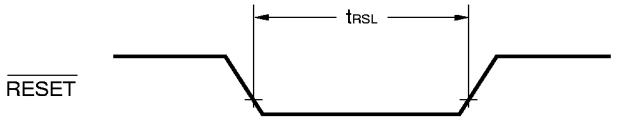
Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



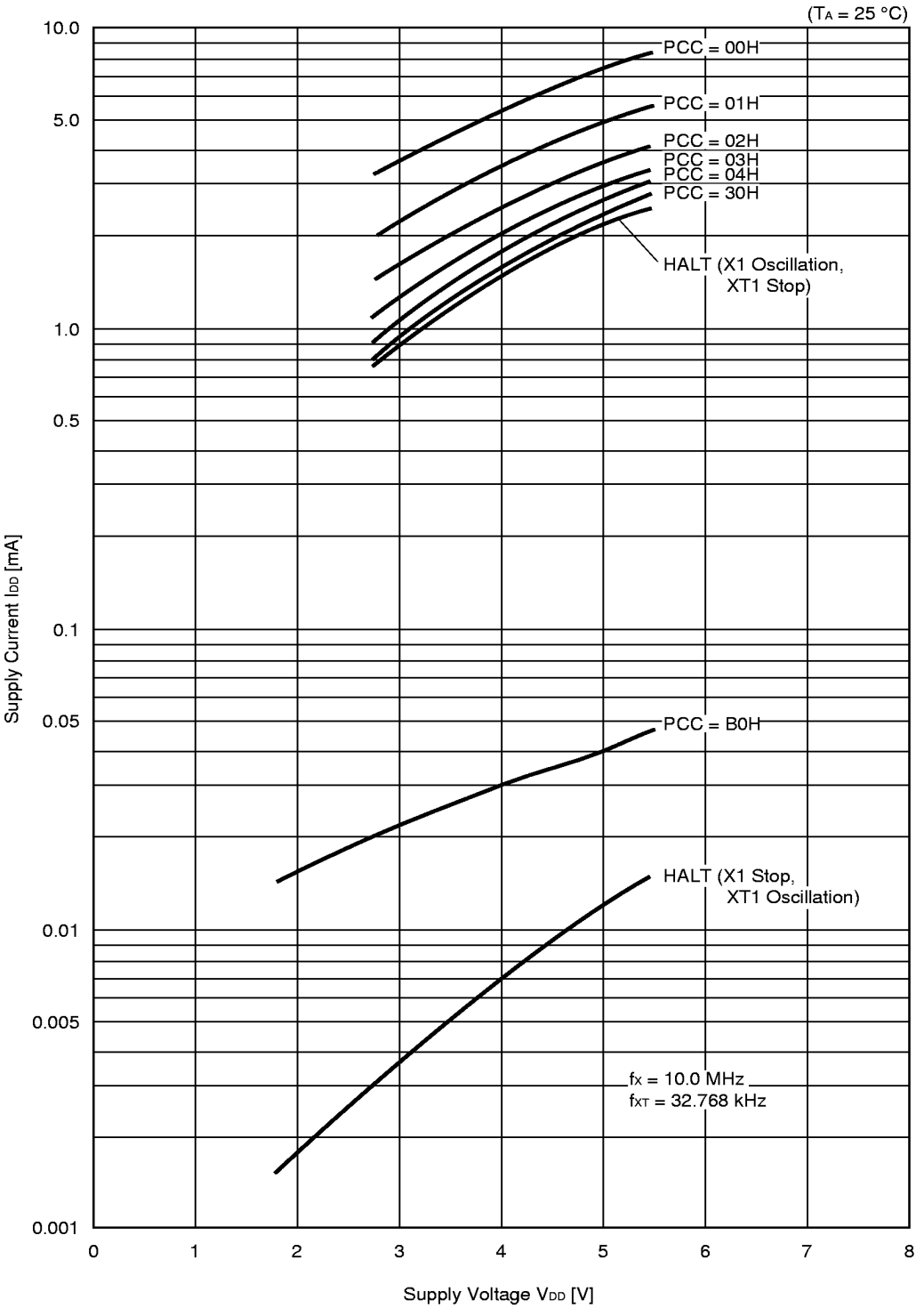
$\overline{\text{RESET}}$ Input Timing



12. CHARACTERISTIC CURVE (REFERENCE VALUES)

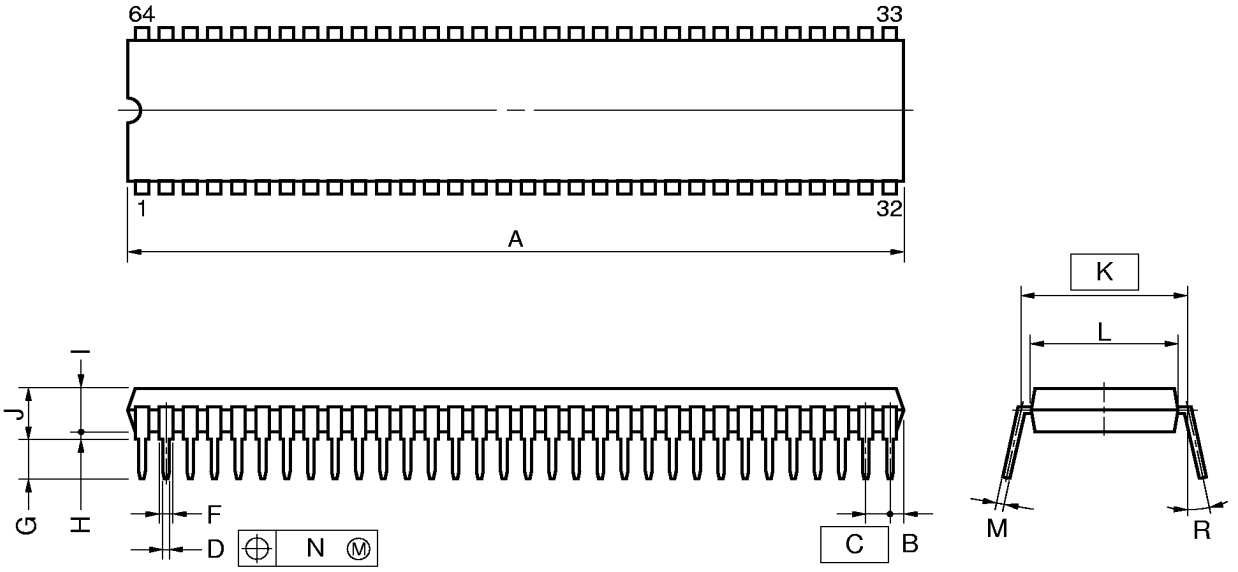
● **Characteristic Curve of μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A)**

I_{DD} vs V_{DD} (Main System Clock: 10.0 MHz)



13. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

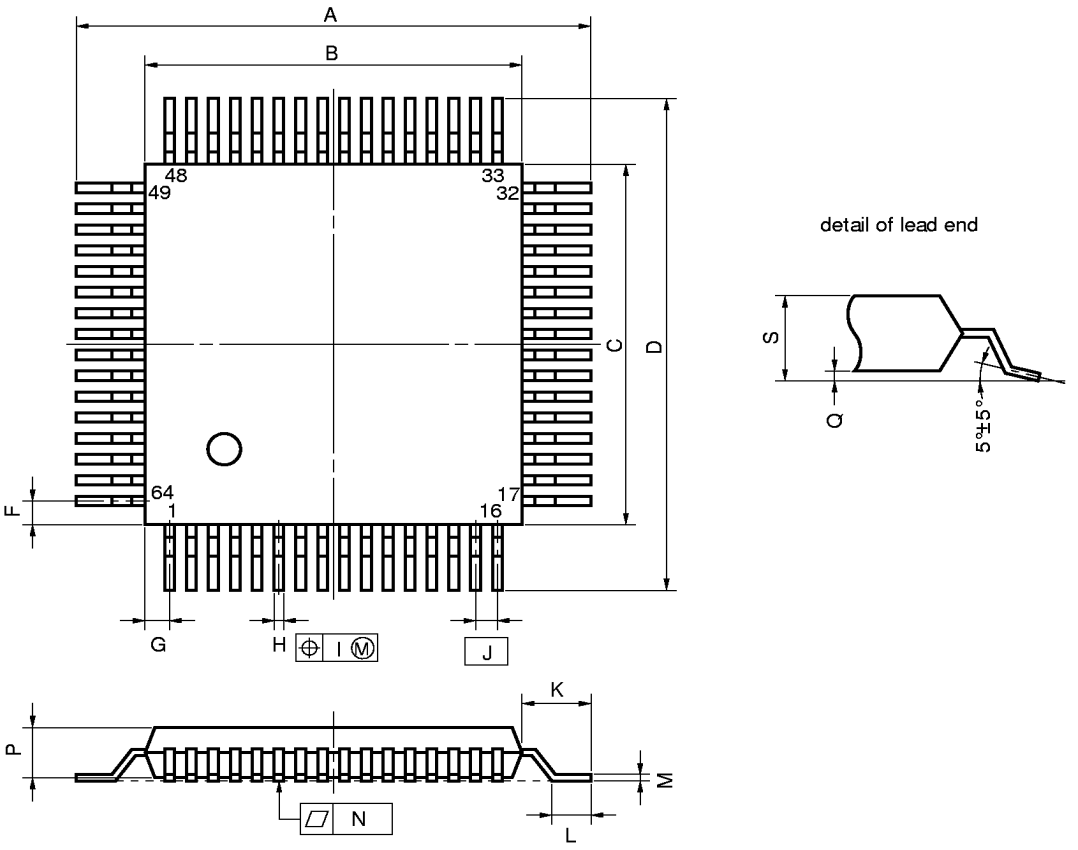
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Remark Dimensions and materials of ES products are the same as those of mass-production products.

64 PIN PLASTIC QFP (□14)



P64GC-80-AB8-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Remark Dimensions and materials of ES products are the same as those of mass-production products.

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78011F(A)/78012F(A)/78013F(A)/78014F(A)/78015F(A)/78016F(A) and 78018F(A) should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our salespersonnel.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD78011FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78012FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78013FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78014FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78015FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78016FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78018FGC(A)-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
★ **μPD78012FGC(A2)-×××-AB8: 64-Pin Plastic QFP (14 × 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Caution Use more than one soldering method should be avoided (except in the case of partial heating).

Table 14-2. Insertion Type Soldering Conditions

μPD78011FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)
μPD78012FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)
μPD78013FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)
μPD78014FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)
μPD78015FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)
μPD78016FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)
μPD78018FCW(A)-×××: 64-Pin Plastic Shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

Caution Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78018F subseries.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 series common C compiler package
DF78014 Notes 1, 2, 3, 4	μPD78014 subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 series common C compiler library source file

PROM Writting Tools

PG-1500	PROM programmer
PA-78P014CW PA-78P018GC	Programmer adapter connected to PG-1500
PG-1500 controller Notes 1, 2	PG-1500 control program

Debugging Tool

	IE-78000-R	78K/0 series common in-circuit emulator
★	IE-78000-R-A	78K/0 series common in-circuit emulator (integrated debugger)
	IE-78000-R-BK	78K/0 series common break board
	IE-78014-R-EM-A	μPD78018F and 78018FY subseries evaluation emulation board (V_{DD} = 3.0 to 6.0 V)
	EP-78240CW-R EP-78240GC-R	Emulation probe common to μPD78244 subseries
	EV-9200GC-64	Socket to be mounted on target system board created for the 64-pin plastic QFP (GC-AB8 type)
	SM78K0 Notes 5, 6, 7	78K/0 series common system simulator
	ID78K0 Notes 4, 5, 6, 7	IE-78000-R-A integrated debugger
	SD78K/0 Notes 1, 2	IE-78000-R screen debugger
	DF78014 Notes 1, 2, 4, 5, 6, 7	Device file common to μPD78014 subseries

Real-Time OS

RX78K/0 Notes 1, 2, 3, 4	78K/0 series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 series OS

Fuzzy Inference Devleopment Support System

FE9000 Note 1/FE9200 Note 6	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and compatible (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™, (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

Remarks 1. For development tools manufactured by a third party, refer to the **78K/0 Series Selection Guide (U11126E)**.
2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF78014.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

	Document Name		Document No.	
			Japanese	English
	μPD78018F, 78018FY Subseries User's Manual		U10659J	U10659E
	μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) Data Sheet		U11921J	This document
★	μPD78P018F(A) Data Sheet		U12132J	U12132E
★	78K/0 Series User's Manual - Instruction		U12326J	IEU-1372
	78K/0 Series Instruction List		U10903J	—
	78K/0 Series Instruction Set		U10904J	—
	μPD78018F Subseries Special Function Register List		IEM-5594	—
	78K/0 Series Application Note	Fundamental (I)	IEA-715	IEA-1288
		Floating-Point Arithmetic Program	IEA-718	IEA-1289

Development Tools Documents (User's Manual) (1/2)

	Document Name		Document No.	
			Japanese	English
	RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
		Language	EEU-815	EEU-1404
	RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
★	RA78K0 Assembler Package	Operation	U11802J	U11802E
		Language	U11801J	U11801E
		Structured Assembly Language	U11789J	U11789E
	CC78K Series C Compiler	Operation	EEU-656	EEU-1280
		Language	EEU-655	EEU-1284
★	CC78K0 C Compiler	Operation	U11517J	U11517E
		Language	U11518J	U11518E
	CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
★	CC78K Series Library Source File		U12322J	—
★	PG-1500 PROM Programmer		U11940J	EEU-1335
	PG-1500 Controller PC-9800 Series (MS-DOS) Base		EEU-704	EEU-1291
	PG-1500 Controller IBM PC Series (PC DOS) Base		EEU-5008	U10540E
	IE-78000-R		EEU-810	U11376E
	IE-78000-R-A		U10057J	U10057E
	IE-78000-R-BK		EEU-867	EEU-1427
	IE-78014-R-EM-A		EEU-962	U10418E
	EP-78240		EEU-986	EEU-1513

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Development Tools Documents (User's Manual) (2/2)

	Document Name		Document No.	
			Japanese	English
	SM78K0 System Simulator Windows Base	Reference	U10181J	U10181E
★	SM78K Series System Simulator	External Components User Open Interface Specification	U10092J	U10092E
	ID78K0 Integrated Debugger EWS Base	Reference	U11151J	—
★	ID78K0 Integrated Debugger PC Base	Reference	U11539J	U11539E
★	ID78K0 Integrated Debugger Windows Base	Guide	U11649J	U11649E
★	SD78K/0 Screen Debugger	Introduction	EEU-852	U10539E
	PC-9800 Series (MS-DOS) Base	Reference	U10952J	—
	SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
	IBM PC/AT (PC DOS) Base	Reference	U11279J	U11279E

Embedded Software Documents (User's Manual)

	Document Name		Document No.	
			Japanese	English
	78K/0 Series Real-Time OS	Fundamental	U11537J	—
		Installation	U11536J	—
★	78K/0 Series OS MX78K0	Fundamental	U12257J	—
	Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
	78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
	78K/0 Series Fuzzy Inference Development Suport System - Fuzzy Inference Module		EEU-858	EEU-1441
	78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

	Document Name	Document No.	
		Japanese	English
	IC Package Manual	C10943X	
	Semiconductor Device Mounting Technology Manual	C10535J	C10535E
★	Quality Grades on NEC Semiconductor Device	C11531J	C11531E
	NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
	Electrostatic Discharge (ESD) Test	MEM-539	—
	Guide to Quality Assurance for Semiconductor Device	C11893J	MEI-1202
	Guide for Products Related to Microcomputer: Other Companies	U11416J	—

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